Design and Fabrication of Bond Pads for Flip-Chip Bonding of Custom Dies to CMOS Dies

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1. Scope

This application note covers the following topics:
- Flip-chip bonding of a custom fabricated die to a standard CMOS die;
- Design of bond pads, mainly top surface metallurgy, for the custom die;
- Fabrication of bond pads, focusing on metal deposition by wet plating;
- Case study related to a vertically-integrated image sensor prototype.

2. Background

At the University of Alberta, the Imaging Science Lab aims to develop vertically-integrated (VI) CMOS image sensors with capabilities that exceed those of conventional CMOS image sensors. VI-CMOS image sensors are examples of 3D electronics because they consist of photodetectors that are placed in a layer above standard CMOS circuits. Although metal lines commonly pass over transistors in CMOS image sensors, a distinguishing characteristic of VI-CMOS image sensors is the layering of semiconductor devices. The main advantage of vertical integration is that the different layers may be fabricated using different processes, each one optimized to best suit the type of devices it contains.

VI-CMOS image sensors may be made using thin-film-on-ASIC (TFA) [1], flip-chip [2], or through-silicon-via (TSV) technology [3]. TFA and TSV technology are difficult without whole CMOS wafers and, therefore, are not practical with CMC multi-project wafers, where clients receive CMOS dies only (at a relatively low cost). Consequently, we are developing a VI-CMOS image sensor prototype using flip-chip technology. However, TFA and TSV technology may prove more economical for mass production of VI-CMOS image sensors.

3. Description of Application

The VI-CMOS image sensor prototype is composed of two dies: a silicon die with CMOS circuits and a glass die with photodetectors. Flip-chip bonding provides both electrical and mechanical connection between the two. The silicon die has been fabricated using a standard CMOS process at DALSA. The glass die has been fabricated using a custom process, involving the University of Alberta Nanofab and Micralyne. With flip-chip bonding, the two dies are
aligned precisely and attached with metallic interconnects. A drawing of the prototype is given in Figure 1.

Figure 1. a. Drawing of a VI-CMOS image sensor prototype. Light enters from the back of the flipped glass die and travels through the glass before reaching an array of photodetectors. Thinner glass substrates and wider image sensors are possible but the drawing shows relative dimensions of an actual prototype. b. Schematic of the glass die with photodetectors. Indium tin oxide (ITO) is deposited on Borofloat glass. The transparent ITO forms a common electrical contact to all photodetectors. Hydrogenated amorphous silicon (a-Si:H) is deposited on the ITO. The photosensitive a-Si:H is etched at the periphery. Bond pads are required on the a-Si:H and ITO regions to enable flip-chip bonding of the glass die to the silicon die with CMOS circuits.

To assemble the prototype, both of the dies described above require pre-processing for flip-chip bonding. Because the CMOS die is fabricated in a standard way, it may also be pre-processed for flip-chip bonding in a standard way. For the glass die, because it is fabricated in a custom way, one needs to determine the best way to pre-process it for flip-chip bonding. Consequently, this application note begins with the design and fabrication of bond pads for a custom die in general, but ends with the most suitable approach for our glass die in particular.

4. Design of Bond Pads

There are several approaches to flip-chip assembly of two dies. Bonding can be done using solder bumps, gold stud bumps, or conductive adhesives (polymer films that contain metallic particles) [4, 5]. This application note focuses on flip-chip bonding using solder bumps.

Flip-chip bonding of two dies using solder bumps requires pre-processing of both dies, as illustrated in Figure 2. Under bump metallization (UBM), also called ball-limiting metallurgy (BLM), is required on the bond pads of one die, which may be called “the main die”. This is followed by the fabrication of solder bumps on the UBM. Top surface metallurgy (TSM) is required on the bond pads of the other die, which is usually called “the substrate”.
Figure 2. Pre-processing required for flip-chip bonding (not drawn to scale). Metal layers, which form the UBM, are deposited on the bond pads of the main die (a silicon die with CMOS circuits in our case). Solder bumps, tens of microns thick, are fabricated on the UBM. Other metal layers, which form the TSM, are deposited on the substrate (a glass die with photodetectors in our case). Although this application note focuses on the TSM, similar principles apply to the UBM.

Bonding quality depends on the solder material and the bond pad metallurgy. We describe the soldering process and commonly used solders below. Thereafter, we explain the metallurgical principles essential for proper design of the TSM, focusing on the vertical profile of the bond pads. Horizontal profiles are not discussed, except to say that the minimum pad footprint and the minimum distance between adjacent pads are specified by the flip-chip bonding supplier.

4.1. Solder Material

Before soldering, two mating surfaces may need to be cleaned using flux. Then, molten filler is used to wet the two surfaces to form a metallurgical bond [6]. Unlike welding, the parts joined by soldering are expected to remain solid during the bonding process. Therefore, the melting temperature of the filler metal or alloy must be lower than that of the parts to be assembled.

Most of the fillers, or solders, used for flip-chip bonding are tin-based or indium-based alloys [4]. Mixtures of tin or indium with lead are commonly used although there has been a tendency to minimize or eliminate the lead in solders recently [7]. Nonetheless, lead-tin solders have superior wetting and spreading characteristics in comparison to most other solders, including indium-based ones. Both tin and lead are inexpensive metals, and the mechanical properties of lead-tin solders are satisfactory. However, tin-based solders form brittle compounds with copper and gold, which are metals commonly used with semiconductor devices [6]. These compounds may crack, leading to joint failure [4].

Indium-based solders are recommended when bonding substrates are coated with gold because the solubility of gold in these solders is much lower than the solubility of gold in lead-tin solders [6]. Furthermore, the formation of a gold-indium alloy suppresses any further reactions between
these two metals. The low melting point of solder alloys with high indium composition makes them suitable for applications where exposure to high temperature is not desired (e.g., organic substrates). However, lead-indium joints are more vulnerable to humidity than lead-tin joints [8]. To prevent corrosion, they need better protection from the environment.

4.2. Top Surface Metallurgy

Bond pads may be designed for metal or nonmetal substrates. Nonmetals, such as semiconductors, ceramics, and polymers, are usually chemically stable. These materials normally do not bond well with molten solder, unless the solder is tailored to react with negatively charged particles, such as oxygen and nitrogen ions, found in the nonmetal substrate or its surface [6]. In general, when standard solders are used, nonmetal substrates must be metallized with TSM to provide a wettable surface for the solder. Metal substrates that cannot be wetted by the molten solder also require TSM. In this application note, we focus on nonmetal substrates.

Besides having a low resistance, the TSM needs to adhere well to the substrate while providing good wettability to the solder. No single metal layer can meet both requirements. Therefore, the TSM is composed of several metal layers, which we describe below.

4.2.1. Foundation Layer

For good adhesion of the TSM to a nonmetal substrate, the foundation (or adhesion) layer that directly contacts with the substrate must be a reactive metal [6]. Reactive metals have a strong affinity to oxygen. They form strong bonds with clean surfaces of nonmetals that contain oxygen or that have surface oxides. Chromium and titanium are good choices for many substrates.

When choosing the foundation layer, one must also consider diffusion rates of the metal atoms into the nonmetal substrate, and the influence of the former on the latter. For example, iron has a strong affinity to oxygen and, therefore, a good adhesion to nonmetal substrates [9]. However, iron must not be used as a foundation layer for silicon devices. Because iron is a middle band-gap dopant in silicon [10], it forms trap states in the semiconductor that increase leakage currents and degrade device performance. Gold, silver, nickel, and copper are also middle band-gap dopants in silicon.

4.2.2. Barrier Layer

The TSM may require a barrier layer to prevent metallurgical reaction between the foundation layer and the wettable layer. Gold, which is a popular choice for the wettable layer, diffuses into some reactive metals, including chromium [11] and titanium [12], to form intermetallic compounds [13]. Presence of gold in the foundation layer can result in the diffusion of gold atoms into the nonmetal substrate, which may be undesirable (see Section 4.2.1). Furthermore, the formation of an alloy between the foundation and wettable layers may decrease the overall wettability of the TSM to solder and increase the brittleness of the solder joint.

The barrier layer may be either a pure metal or an alloy. Platinum, nickel, copper, titanium-tungsten alloy, and titanium nitride are commonly used as the barrier [6]. The layer must be thick enough to survive flip-chip bonding. It must also block the unwanted diffusion of TSM atoms.
sufficiently, while maintaining a good conductivity, for the expected lifetime of the assembled device.

4.2.3. Wettable Layer

There are two thermodynamic principles that determine whether the surface of a solid substrate can be wetted by a droplet of liquid solder. They are the Young-Dupre law and the Gibbs function [14].

According to the classical model of wetting, a liquid droplet reaches equilibrium with a solid substrate when the three components of surface tension—\( \gamma_{SL}, \gamma_{LV}, \) and \( \gamma_{SV} \)—are in balance, as shown in Figure 3. The relationship between these forces and the contact angle, \( \theta \), is expressed by the Young-Dupre law, \( \cos \theta = (\gamma_{SV} - \gamma_{SL})/\gamma_{LV} \), which is also known as the wetting equation. When \( 90^\circ < \theta < 180^\circ \), the liquid does not spread on the surface, although there is contact between the droplet and substrate. When \( \theta < 90^\circ \), the liquid spreads on the surface, and the substrate is said to be wetted by the liquid [6].

![Figure 3. A liquid droplet spreads on a solid substrate until three surface tension forces are in balance: the tension \( \gamma_{SL} \) between the solid substrate and the liquid droplet; the tension \( \gamma_{LV} \) between the liquid droplet and the (vapour) atmosphere; and the tension \( \gamma_{SV} \) between the substrate and the atmosphere. a. For acute contact angles, the liquid wets the surface. b. For obtuse angles, e.g. due to surface oxidation, the liquid does not wet the surface.](image)

Gibbs function implies that when a spontaneous change occurs on a surface, the surface free energy is lowered. Consequently, formation of a thin oxide layer on the surface would decrease \( \gamma_{SV} \) and increase \( \theta \), which would reduce the liquid’s ability to wet the substrate [14]. For this reason, the reactive metal in the foundation layer of the TSM would lose its wettability once exposed to the atmosphere. To overcome this problem, a more noble metal, which offers good wettability to the solder, must be deposited on the foundation layer. This wettable layer must be sufficiently thick to protect the underlying metal layers from corrosion and to maintain wettability of the component over a reasonable shelf life prior to soldering [6].

Because gold resists oxidation, it is commonly used as the outermost layer in the TSM for fluxless soldering [14]. Gold can be used as a protective coating to the wettable layer or it can be used as the wettable layer itself. In the former case, a thin gold layer is required, and the solder is a material into which gold quickly dissolves to expose the underlying wettable layer to the solder. Commonly used materials are nickel, as the wettable layer underneath the gold, and a tin-based solder, usually lead-tin. In the latter case, a solder material in which gold has low solubility is desired. Commonly used solders are indium-based, usually lead-indium.
5. Fabrication of Bond Pads

Bond pad fabrication can either be done in house, as additional steps to the preparation of custom dies, or be outsourced to an external supplier. With outsourcing, bond pad design remains important, especially for custom dies, and some understanding of fabrication is essential for successful design. Due to our proximity to the University of Alberta Nanofab, it was convenient for us to explore some design choices by fabricating the bond pads ourselves.

There are four basic methods to deposit metal layers on metallic and nonmetallic substrates: physical vapour deposition (PVD), chemical vapour deposition (CVD), wet plating, and thick-film metallization. This section covers PVD and wet plating because they are the only metal deposition methods currently available at the Nanofab and at CMC.

Although flip-chip bonding is done in this application with dies, it is easier and cheaper to fabricate the bond pads on whole wafers, and to dice them as the last step before the flip-chip bonding.

5.1. Physical Vapour Deposition

In PVD, material particles are brought into the vapour phase prior to deposition on a nearby substrate surface. The relatively slow deposition rate of PVD limits its usefulness mainly to thin film fabrication, with thicknesses up to a few hundred nanometers.

5.1.1. Evaporation

The material to be deposited is thermally vapourized under high vacuum conditions. Common methods to achieve the vapourization are resistance heating and electron beam bombardment.

5.1.2. Sputtering

A target made of the material to be deposited is bombarded with ions of an inert gas, usually argon. As a result of momentum transfer between the ions and the target, atoms are released from the latter. Sputter guns with magnetrons enhance ion generation close to the target. This increases the deposition rate of atoms on the nearby substrate and, in general, makes the process more efficient.

5.1.3. Difficulties

Using the Lesker magnetron sputtering machines at the University of Alberta Nanofab, we tried to deposit thick films (500 nm or more) of aluminum and nickel to serve as metal layers for bond pads. However, the films were of poor quality. The aluminum looked cloudy or white instead of the usual shiny metallic colour, which could be obtained by sputtering thin films instead. As for the nickel, its surface was cracked and it could not be etched by conventional nickel etchants.

We suspect that during a long deposition time, which is required for thick films, the sputter chamber warms up, resulting in excessive outgassing. Gases trapped within surfaces inside the chamber, which is initially at room temperature, may not be pumped out during a pump-down step that is done prior to deposition. As the temperature rises during a long deposition, the gases
may obtain enough energy to escape into the chamber while the deposition is proceeding. These outgassed particles are impurities that would contaminate the deposited films, thereby changing their characteristics.

5.2. Wet Plating

In wet plating, a metal layer is deposited by immersion of the substrate in a liquid, which contains the appropriate metallic ions. Electroless plating and electroplating have a relatively high deposition rate, and are therefore suitable for thick film fabrication, with thicknesses up to a few microns. However, control on the thickness of the deposited film is less precise than with PVD.

All wet plating methods use the electrochemical mechanisms of oxidation and reduction. Both reactions involve the transfer of electrons between reacting substances. Oxidation is characterized by a loss of electrons or “de-electronation”, while reduction is characterized by a gain of electrons or “electronation” [15]. Electroplating requires an external power source. However, electroless plating and immersion plating do not require any electrical circuitry.

5.2.1. Electroplating

Electroplating uses an electrolytic cell that consists of two electrodes submerged in a solution containing ions. A current is passed between the anode and cathode. Unlike electronic circuits, which use electrons to carry a current, the electrolytic cell uses ions to carry a current.

The sample or piece to be plated is connected to the cathode. There are two types of anodes: sacrificial anodes and permanent anodes [15]. Sacrificial anodes are made of the metal to be deposited. They supply the solution with fresh ions of the metal to replace the ions consumed during the plating. Permanent anodes serve only to complete the electrical circuit. In this case, the anode is not consumed during electroplating and the amount of ions in the solution decreases with time.

When a DC current is passed between the electrodes, positively charged metal ions in the solution are attracted to the sample at the cathode, which is negatively charged. The metal ions absorb electrons from the cathode, undergoing a reduction process that transforms them into metal atoms. These atoms are deposited on the sample surface and form the plated film. Non-uniformity of the current density over the sample leads to non-uniformity in the thickness of the deposited film. Current density is higher at or near the edges and corners of the sample.

To ensure the electroplated metal adheres well to a substrate surface, a good seed layer is required. The seed layer is usually a thin metal layer (100 to 200 nm thick) that does not oxidize easily. Gold, copper, and nickel are commonly used for this purpose. Figure 4 depicts the result of an early electroplating trial. We tried to electroplate nickel onto glass substrates coated with a sputtered layer of chromium. Because the chromium oxidized easily in standard room conditions, it proved unsuitable as a seed layer. The electroplated nickel did not adhere to the substrate surface and could be peeled off easily, as shown in Figure 4.
5.2.2. Electroless Plating

With electroless plating, or autocatalytic plating, a chemical reducing agent is placed in the solution together with ions of the metal to be deposited. The deposition only occurs on catalytic surfaces. Not only must the initial surface be catalytic, but the deposited metal must also be a catalytic surface for the deposition process to continue.

In comparison to electroplating, electroless plating may be done on surfaces of non-conductive materials, although the surfaces may need pre-processing to make them catalytic for the reaction. Another advantage of electroless plating is that metal is deposited uniformly. There is no excessive buildup at or near edges and corners. The main disadvantage of electroless plating is that the reducing agents are usually more expensive as electron sources compared to electron currents [15].

5.2.3. Immersion Plating

Like electroless plating, immersion plating does not require an external circuit. However, there is no reducing agent in the solution. Instead, metal atoms from the original surface of the immersed sample undergo an oxidation process, which releases them as ions into the solution. These atoms are replaced by other ions in the solution that undergo a reduction process, which deposits them on the sample as metal atoms. The process works only if the metal to be deposited is more noble (i.e., has a lower oxidation potential) than the original metal on the sample surface [16].

A combination of electroless nickel and immersion gold (ENIG) is commonly used to fabricate bond pads for soldering. Surface nickel atoms from the electroless plating are replaced with gold atoms during the immersion plating. Deposition proceeds until a thin layer of gold covers the nickel.
6. Case Study: Bond Pads on Coated Glass

The previous sections discussed general principles related to the design and fabrication of bond pads for flip-chip bonding of custom dies to CMOS dies. We revisit these principles here for a specific case study, namely the development of a prototype VI-CMOS image sensor (see Figure 1). The custom die is a glass die on which a photodetector array has been fabricated. To complete the VI-CMOS image sensor, it must be flip-chip bonded to a silicon die containing CMOS read-out circuits.

Bond pads are required on the custom die, which is actually not a glass substrate. To make the photodetector array, the glass has been coated with ITO and a-Si:H. The ITO, which is a transparent conductor, forms a front electrical contact to all photodetectors in the a-Si:H, which is a semiconductor. Because the a-Si:H is not patterned, the array of photodetectors is defined by the array of bond pads fabricated on the a-Si:H. These bond pads form the back electrical contacts of all photodetectors, with respect to light entering the image sensor. Bond pads must also be fabricated on the ITO, at the periphery of the photodetector array, to establish a connection between the front electrical contact and the CMOS die.

6.1. Design of Bond Pads

Our application required the design of bond pads for a-Si:H and ITO substrates. Due to the initial capabilities of the flip-chip bonding suppliers to whom we had access, our pads had a footprint of 55 × 55 µm² and a centre-to-centre spacing of 110 µm. These dimensions determine the horizontal profiles of the UBM, on the CMOS dies, and the TSM, on the glass dies (see Figure 2). They also define our pixel size, which is large for a visible-band image sensor.

Because the standard CMOS dies were to be pre-processed for flip-chip bonding by a third party, we focused on the pre-processing of the custom glass dies, in other words on the TSM. For the foundation layer of the TSM, we chose 100 nm of sputter-deposited chromium. Chromium was preferred over titanium because our titanium etchant contained hydrofluoric acid (HF). Since HF also etched glass, it was not suitable for coated glass substrates. The chromium showed good adhesion to the a-Si:H and ITO substrates, as well as the naked glass substrates.

As for the wettable layer of the TSM, we considered three options, which are presented in succeeding sections along with our final design.

6.1.1. Option 1: Electroless Nickel and Immersion Gold

In this case, the nickel is the wettable layer for soldering, and the gold is there to prevent oxidation of the nickel when the TSM is heated as a preparation for bonding. Lead-tin solder is used. This process cannot be done in the University of Alberta Nanofab, but it is available through CMC. We were asked to prepare bond pads with aluminum layers several microns thick to serve as the initial catalyst for the electroless nickel. Currently, aluminum deposition in the Nanofab can be done only by sputtering. Because thick films of sputtered aluminum proved to be of poor quality (see Section 5.1.3), this option was not suitable for us.
6.1.2. **Option 2: Electroplated Nickel and Electroplated Gold**

A thick nickel layer (several microns) and a thin gold layer (several hundred nanometers) are deposited by electroplating in this case. The roles of the nickel and gold layers are the same as in Option 1. Similarly, lead-tin solder is used. To ensure adhesion of the electroplated nickel, a seed layer needs to be deposited on the chromium foundation layer (see Figure 4). Moreover, two stages of electroplating are required, which increases the complexity of the process.

6.1.3. **Option 3: Electroplated Gold**

In this case, a thick layer of electroplated gold (about 1.5 µm) is used as the wettable layer. Indium-based solder bumps are then used (lead-indium was available from the flip-chip supplier). Compared to Option 2, it may seem that using a thick gold layer costs more. However, considering the protocol of electroplating at the Nanofab, and the small scale of our prototype, the actual cost is economical.

6.1.4. **Final Design**

We decided to use chromium as the foundation layer and gold as the wettable layer (Option 3). For the electroplating of gold, we used nickel as a seed layer. A thin nickel layer can be deposited by sputtering immediately after the sputter deposition of chromium, and nickel can be etched with chemicals that are available in the Nanofab. Unlike sputtered platinum or gold, which can also be used as a seed layer for electroplated gold, nickel is relatively inexpensive. Also, nickel serves as a good barrier layer between gold and chromium. The final design of the bond pads was a 100 nm foundation layer of chromium, a 200 nm barrier/seed layer of nickel, and a 1.5 µm wettable layer of gold.

6.2. **Fabrication of Bond Pads**

Figure 5 illustrates the main process steps in the fabrication of bond pads on the a-Si:H and ITO regions of the glass substrates. These bond pads enable our custom dies to be flip-chip bonded with CMOS dies. All steps were done at the University of Alberta Nanofab.
Figure 5. Fabrication of bond pads: 1. Sputtering of a 100 nm foundation layer of chromium and a 200 nm barrier/seed layer of nickel. 2. Lithography—only the areas that will be bond pads are exposed. 3. Electroplating of a 1.5 µm wettable layer of gold. Deposition occurs only on the exposed nickel, which is connected to the cathode. 4. Stripping of the photoresist. 5. Etching of the nickel and chromium, except from underneath the gold.
1. Sputtering of chromium and nickel: This step was done in a Lesker DC magnetron sputtering machine. Both materials were sputtered at 300 W, in an argon atmosphere at 7 mTorr.

2. Lithography: After this step, the whole substrate was covered with photoresist, except for the $55 \times 55 \, \mu m^2$ squares that would define the bond pads. Only one mask was required.

3. Electroplating of gold: Using a Techni Gold 25 E S solution, deposition was done at 40 °C. The current density was about 0.1 ASD (Amperes per square decimeter), and the deposition rate was about 65 nm/min. Figure 6 depicts the Nanofab station developed through this work.

4. Stripping of the photoresist: After washing residues of the electroplating solution from the sample, the photoresist was stripped using acetone and IPA (isopropyl alcohol).

5. Etching of the nickel and chromium: First, the nickel was etched using a diluted solution of FeCl$_3$. Next, the chromium was etched using a chromium etchant solution. The gold acted as a mask.

Photos of the finished glass dies, prior to dicing, are given in Figure 7. The size of each bond pad is $55 \times 55 \, \mu m^2$. In the a-Si:H photodetector array, the distance between the centres of two adjacent bond pads is 110 µm. The size of each die, excluding the dicing lines, is $3.7 \times 3.3 \, mm^2$. Each die represents one half of a VI-CMOS image sensor prototype.
7. Conclusion

This application note describes the design and fabrication of bond pads on custom dies so that they can be flip-chip bonded to CMOS dies. Design of bond pads entails top surface metallurgy and solder materials. With nonmetal substrates, such as semiconductors, the bond pads have to be composed of several metal layers. The foundation layer must be reactive but the wettable layer must resist oxidation. Fabrication of bond pads involves wet plating and physical vapour deposition. Electroplating and electroless plating are suitable ways to make thick metal layers; whereas, sputtering and immersion plating are suitable for making thin metal layers.

We used sputtering and electroplating to fabricate bond pads on coated glass substrates. The design included a chromium foundation layer and a gold wettable layer. This specific example of the general approach to bond pads is taken from a vertically-integrated image sensor prototype, which we will complete using flip-chip bonding.

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9. References


