

**UNIVERSITY OF ALBERTA**

**DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING**

**ECE 512 – Digital System Testing and Design for Testability**

**Midterm Examination**

Instructors: B. F. Cockburn  
Exam date: October 30, 2009  
Exam duration: 50 minutes  
Aids permitted: Hardcopies of the course overheads as well as the course textbook.  
Electronic calculators are permitted.

Instructions:

1. Fill out your printed name, signature and I.D. number on this page.
2. Verify that this booklet contains 6 pages.
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for rough work.

**Student name:** \_\_\_\_Model Solutions\_\_\_\_

**Signature:** \_\_\_\_\_

**Student I.D.:** \_\_\_\_\_

<b>Question</b>	<b>Time</b>	<b>Worth</b>	<b>Mark</b>	<b>Subject</b>
1.	10	20		Basic Testing Concepts
2.	10	20		Automatic Test Equipment
3.	10	20		Testability Analysis
4.	10	20		PODEM
5.	10	20		Muth's Nine-Valued Logic
<b>Total</b>	<b>50 mins</b>	<b>100</b>		--

## Question #1 (Basic Testing Concepts)

- (a) Design-for-testability techniques allow product quality to be increased and testing costs to be reduced over the lifetime of an electronic system. What are the major additional costs associated with providing design-for-testability features in an integrated circuit design?
- Increased IC design costs, including more design verification costs
  - Cost of additional test engineers
  - Increased hardware (e.g. more silicon area per IC)
  - Reduced hardware performance (e.g. due to extra multiplexers and the extra capacitance introduced by the test circuitry)
  - Decreased chip yield due to larger ICs
- (b) In the modern marketplace for integrated circuits, customers expect defect levels of less than 500 ppm. Why does this imply that the coverage of single stuck-at faults be well over 99%? In your answer, be sure to explain the difference between physical defects and stuck-at faults.
- If the defect level is to be less than 500 parts per million = 0.05%, the defect coverage will be greater than 99.95%.
  - But the stuck-at fault coverage of tests for most ICs correlates quite closely (but not perfectly) with the defect coverage of the tests, so the stuck-at fault coverage will also have to be at least 99.95%.
  - Many, but not all, physical defects cause behaviour that corresponds to the stuck-at fault model. But a test that detects all stuck-at faults forms a screen that has proven, through industrial experience, to be effective at finding a wide variety of faulty behaviours caused by physical defects.
  - A physical defect describes an out-of-spec physical structure that disturbs the behaviour of a circuit. A fault model is a convenient description of faulty behaviour (e.g. a line is stuck-at-0 or 1).

## Question #2 (Automatic Test Equipment)

- (a) What is the "test head" of an integrated circuit tester? Why does the cost of the test head typically account for a large fraction of the total cost of a tester?
- The test head, although relatively small in size, contains a large number of densely populated pin electronics cards. These cards contain a large fraction of the electronics required for pin connections to the IC under test.
- (b) Describe what is meant by a "DC parametric test"? Give two examples of different DC parametric tests to support your answer.
- A DC parametric test is a measurement of a steady-state analog parameter, such as a current or voltage.
  - A continuity test sinks or sources a current to an input pad, and determines whether or not the resulting voltage drop is consistent with a protection diode being present in the chip pad circuit.
  - An input threshold test determines the maximum input voltage that is sensed as a logic 0, or the minimum input voltage that is sensed as a logic 1.
  - There are many other kinds of DC parametric tests.
- (c) Describe what is meant by an "AC parametric test"? Give two examples of different AC parametric tests to support your answer.
- An AC parametric test is a measurement of an analog circuit characteristic as the circuit signals change in response to a change in the input signals.
  - A propagation delay test measures the time interval between the instant when an input signal reaches the 50% voltage between the high and low input voltages, and the time instant when a changed output signal reaches the 50% voltage.
  - A maximum operating frequency test determines the maximum clock frequency at which the IC under test can still pass a thorough functional test without errors.
  - There are many other kinds of AC parametric tests.

### Question #3 (Testability Analysis)

- (a) Consider a 3-input majority gate, like the one that was considered in the last question of Assignment #1. Let the inputs be called A, B and C, and let the output be Y. The output Y is 1 if at least two 1's are present at the three inputs. Assume that the controllabilities to 0 & 1 for A are 2 and 3, respectively; for B they are 3 and 5, respectively; and for C they are 3 and 4, respectively. Show how one should compute the controllabilities to 0 & 1 for the output Y, following the same general approach as the SCOAP testability measures.

Controllability of Y to 0 (or 1) is determined by adding 1 (gate cost) to the cheapest way (as a function of the controllabilities of the inputs) of obtaining  $Y = 0$  (or 1) at the majority gate output.

Y=0 for (A,B,C) = (0,0,0) or (0,0,1) or (0,1,0) or (1,0,0)  
Cost of (A,B,C) = (0,0,0) is  $1 + 2 + 3 + 3 = 9$  <- cheapest  
Cost of (A,B,C) = (0,0,1) is  $1 + 2 + 3 + 4 = 10$   
Cost of (A,B,C) = (0,1,0) is  $1 + 2 + 5 + 3 = 11$   
Cost of (A,B,C) = (1,0,0) is  $1 + 3 + 3 + 3 = 10$   
Thus the controllability of Y to 0 is 9.

Y=1 for (A,B,C) = (0,1,1) or (1,0,1) or (1,1,0) or (1,1,1)  
Cost of (A,B,C) = (0,1,1) is  $1 + 2 + 5 + 4 = 12$   
Cost of (A,B,C) = (1,0,1) is  $1 + 3 + 3 + 4 = 11$  <- cheapest  
Cost of (A,B,C) = (1,1,0) is  $1 + 3 + 5 + 3 = 12$   
Cost of (A,B,C) = (1,1,1) is  $1 + 3 + 5 + 4 = 13$   
Thus the controllability of Y to 1 is 11.

- (b) Assuming that the observability of output Y is 7, what would be the observability of input B? Again, use the same general approach as the SCOAP testability measures.

The observability of input B given the observability of Y is given 1 (for the gate) plus the observability of Y plus the cost of the cheapest input combination of (A,B,C) that propagates the value of B to Y.

The input combinations that propagate the value of B to Y are (A,B,C) = (0,B,1) and (1,B,0). The value of B in these two scenarios determines the value of Y.

Cost of observing with (0,B,1) is  $1 + 7 + 2 + 4 = 14$   
Cost of observing with (1,B,0) is  $1 + 7 + 3 + 3 = 14$

Thus the observability of B is 14.

**Question #4 (PODEM)**

<<see the figure in the hardcopy >>>

Consider the combinational circuit shown above. In the space below, construct a matrix that shows how the node signals are progressively determined as a result of executing the PODEM algorithm for a stuck-at-1 fault affecting node “s”. Be sure to label each row with the action type that the algorithm is performing.

Action	a	b	c	d	t	s	e	u	f	y
Initialize	X	X	X	X	X	X	X	X	X	X
Object, s=0										
Backtrace,b=0	X	0	X	X	X	X	X	X	X	X
Forw Implic	X	0	X	X	X	X	X	X	X	X
Backtrace,c=0	X	0	0	X	X	X	X	X	X	X
Forw Implic	X	0	0	0	X	D'	0	X	1	X
Object, t=0										
Backtrace,a=0	0	0	0	0	X	D'	0	X	1	X
Forw Implic	0	0	0	0	0	D'	0	D'	1	D'
Found test!										

### Question #5 (Muth's Nine-Valued Logic)

- (a) Briefly explain the limitations of Roth's five-valued D-algebra when used in fault simulation and test pattern generation for sequential circuits. What exactly goes wrong when this algebra is used with sequential circuits?
- The values in Roth's D-algebra represent pairs of signals; each pair gives the signal in a fault-free circuit and the signal in the faulty circuit.
  - Sequential circuits can have uninitialized memory bit values. The uncertainty created by those bits can propagate through both fault-free and faulty circuits.
  - The only value in Roth's D-algebra for representing this uncertainty is the X value, which requires both the fault-free and faulty circuit values to be unknown.
  - However, detection can occur if there is an output that has 0 or 1 for the fault-free circuit, and X for the faulty circuit. Detection occurs if, because of the state that the circuit powered up in, the faulty circuit happens to have a different value from that of the fault-free circuit.
  - Roth's D-algebra cannot represent these cases of possible detection (0/X and 1/X), and so some probabilistic tests will be impossible to find.
- (b) Briefly describe Muth's nine-valued logic. Be sure to indicate how it is different from the D-algebra. How can Muth's nine-valued logic lead to fault detection in situations where the D-algebra would not indicate fault detection.
- To Roth's 5-valued algebra ( $0 = 0/0$ ,  $1 = 1/1$ ,  $X = X/X$ ,  $D = 1/0$ , and  $D' = 0/1$ ) Muth added the four new values  $0/X$ ,  $1/X$ ,  $X/0$  and  $X/1$ . The convention here is that the value A/B corresponds to value A being present in the good circuit, and value B being present in the faulty circuit.
  - The first of the two new values, if present at an output signal, will lead to detection of the X value in the faulty circuit happens to be different from the 0 or 1 in the good circuit.