UNIVERSITY OF ALBERTA

DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING

ECE 512 – Digital System Testing and Design for Testability

Final Examination

Instructors: B. F. Cockburn
Exam date: December 5, 2008
Exam duration: 60 minutes
Aids permitted: Hardcopies of the course overheads can be freely consulted.
An electronic calculator can be used.

Instructions:
1. Fill out your printed name, signature and I.D. number on this page.
2. Verify that this booklet contains 7 pages.
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for rough work.

Student name: _____

Signature: _____

Student I.D.: _____

Question	Time	Worth	Mark	Subject
1.	10	16		I_{DDQ} Testing
2.	10	16		Test Algebras
3.	10	17		Memory Testing
4.	10	17		Transition Fault Testing
5.	10	17		Test Vector Generation for BIST
6.	10	17		Test Response Compaction
Total	**60 mins**	**100**		--

Question #1 (I_{DDQ} Testing)

(a) In your own words, briefly explain what is meant by I_{DDQ} testing.

(b) What the types of physical defects that are more effectively detected by IDDQ testing than logic level testing?

(c) What are the main technical challenges to be solved when implementing IDDQ testing in a modern integrated circuit?

Question #2 (Test Algebras)

(a) In the context of digital logic testing, what is the D-algebra (also called the D-Calculus)? What is the advantage of using the D-algebra instead of a conventional 2-valued (0 and 1) or a 3-valued (0, 1 and X) algebra?

(b) In the case of sequential logic testing, a 9-valued algebra was introduced by P. Muth. Briefly explain what the values of this algebra mean. Why was it found to be helpful to use this new algebra for testing sequential circuits instead of the D-algebra?

Question #3 (Memory Testing)

(a) The fault models and tests used in memory testing are different in many ways from the fault models and tests used in other digital logic blocks. Briefly explain what it is about memories that makes it necessary to introduce new fault models beyond the familiar stuck-at fault.

(b) Memory tests are frequently design to target the detection of faults in the memory cells, using a so-called reduced functional fault model, even though the memory cells may only occupy 70% or less of the total area of the memory block. Why is it that special tests are not designed to target the detection of faults in the remaining 30% of the memory circuitry?

Question #4 (Transition Fault Testing)

(a) Briefly define what is meant by a “transition fault”.

(b) What are the conditions that must be met by a two-pattern test that detects a particular transition fault (for example, a slow-to-rise transition fault)?

(c) How could one use an Automatic Test Pattern Generation (ATPG) algorithm for stuck-at faults to generate tests for transition faults?

Question #5 (Test Vector Generation for BIST)

(a) Briefly describe the two major types of linear feedback shift registers: external-XOR (standard) LFSRs and inter-XOR (modular) LFSRs. Support your answer by giving the corresponding two 5-bit LFSRs for the following characteristic polynomial:

$$f(x) = 1 + x + x^2 + x^5$$

(b) Briefly explain why LFSRs are used to generate test patterns in built-in self-test designs instead of binary counters.

Question #6 (Test Response Compaction)

Explain why linear feedback shift register (LFSR) based test response compactors are usually used instead of conceptually simpler test response compressors like 1's counters and transition counters. In your answer define what is meant by the term "aliasing". What are the main strategies for controlling aliasing?