Design and Evaluation of a Hybrid Memory Cell by Single-Electron Transfer

Wei Wei, *Student*, Jie Han, *Member* and Fabrizio Lombardi, *Fellow IEEE*

***Abstract*—This paper presents the characterization and design of a Static Random Access Memory (SRAM) cell at nano scale ranges. The proposed SRAM cell incorporates a Single-Electron (SE) turnstile and a Single-Electron Transistor (SET)/MOS circuit in its operation, hence the hybrid nature. Differently from previous cells, the hybrid circuit is utilized to sense (measure) on a voltage-basis the presence of at least an electron as stored in memory, while the turnstile enables the single electron transfer in and out of the storage node. The two memory operations (read and write) are facilitated by utilizing these hybrid circuits; moreover the proposed SRAM cell shows compatibility with MOSFET technology. HSPICE simulation shows that the proposed SRAM cell operates correctly at 45 and 32 nm with good performance in terms of propagation delay, signal integrity, area, stability and power consumption. The extension of the above hybrid design to a Ternary Content Addressable Memory (TCAM) cell is also presented.**

***Index Terms*—Static Random-Access Memory (SRAM), memory cell design, SRAM, single electron transistor (SET), Ternary Content Addressable Memory (TCAM).**

I. INTRODUCTION

CMOS technology is steadily reducing its feature size; scaling at 45 and 32 nm has been used to design advanced high performance electronic systems. However, the reduction in feature size is encountering significant problems as this technology is moving fast toward the end of the roadmap, as predicted by the Semiconductor Industry Association. Emerging technologies have been proposed to supersede the basic CMOS device, i.e. the MOSFET. Examples of emerging technologies are carbon nano tubes, quantum-dot cellular automata, single-electron devices and molecular/magnetic electronics [1] [2] [3] [4]. However, CMOS has evolved over many years and a considerable financial investment has occurred in the fabrication and manufacturing infrastructure of these devices. So, technology changes must be confronted with the economic viability and compatibility of the existing and emerging platforms. It is foreseen that new technologies will be at least initially transitioning through so-called "hybrid" implementations in which CMOS will be still used [5].

Emerging technologies utilize novel physical phenomena in their operation; among them, the Coulomb Blockade (CB) can be utilized for memory devices with the potential of very high capacity and scalability. CB allows considerable electrical margins and low power consumption, because it can control the transfer of individual electrons with extremely small statistical fluctuations. Moreover, it can utilize devices of small dimension [23]. The so-called single-electron (SE) turnstile can be used to sequentially transfer electrons in the circuit node; the turnstile is formed by two voltage-controlled CBs and using two one-dimensional field effect transistors (FETs).

The single-electron transfer transistor (SET) is yet another type of device that has received considerable interest in the technical literature; it is based on measuring either the current or voltage across the transistor. This device however, incurs in a large delay because it suffers from its relatively large output resistance (typical resistance values are in excess of 100 kΩ) and a cable capacitance of at least 1 nF. Today's technology relies on utilizing radio-frequency SETs to reduce delay and improve sensitivity. These fabrication techniques utilize electron beam lithography and standard two-angle evaporation of aluminum with oxidation between the first and second layers for generating tunnel junctions [24]. So, it has been advocated that a SET can be used as a readout device in applications for very sensitive charge meters. For sensing, the device is formed on the same silicon-on-insulator layer for counting the number of transferred electrons and by utilizing processes compatible with those of traditional silicon integrated circuits [24]. These features can also be employed for memory designs with large storage capacity.

SET transistors and circuits are compatible in operation with CMOS and represent viable candidates for implementing hybrid designs [5] [6]. One of the circuits that is fundamental for the adoption of a new technology is the memory cell. The design of an SRAM allows to assessing the performance parameters that are characteristic of an entire technology platform, such as propagation delay and power consumption.

The objective of this paper is to present a novel design of an SRAM cell; this design utilizes a "hybrid" implementation in which SET-based devices are utilized together with CMOS

Manuscript received:06-Mar-2012 revised:24-Oct-2012

W. Wei and F. Lombardi are with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, USA; {lombardi@ece.neu.edu}; J. Han is with the ECE Dept, University of Alberta, Edmonton, Canada {jhan8@ualberta.ca}. This manuscript is an extended version of [26] by the same authors.

.

circuitry to operate an SRAM cell. The proposed memory cell consists of a SE turnstile and a SET/MOS circuit, to respectively transfer and sense (i.e. counting electrons in the storage node); extensive simulation results using HSPICE compatible models [7] [8] are reported at the nano scale feature sizes of 45 and 32 nm. The proposed static memory cell shows good performance metrics such as propagation delay and power consumption. The phase-shift characteristics of the I-V plot are then utilized to efficiently perform the matching operation; hence, a novel Ternary Content Addressable Memory (TCAM) is also proposed. In the proposed design, the matching delay is significantly affected by the matching SET and the internal characteristics of the cell (such as the mechanism of the phase gate for the match outcome when a "Don't Care" value is stored); this mechanism is substantially different from the encoding based operation of a conventional TCAM cell. The proposed design is still hybrid and simulation results show that it is efficient.

This paper is organized as follows. Section II presents a review of the basic circuit elements of a SET memory cell. Section III provides an initial description of the operational modes of the proposed static memory cell. Section IV presents the simulation results of the operational modes. Sections V and VI present a performance assessment of the individual elements and the memory circuit, respectively. The design and evaluation (inclusive of the mechanism of matching by phase-shift) of the proposed TCAM cell are presented in Section VI. Section VII concludes this manuscript.

II. Circuit Elements

A. Single-Electron Turnstile

SE transfer requires the utilization of specific devices, such as pumps and turnstiles. SE pumps and turnstiles have been proposed and experimentally demonstrated by using multiple metal islands separated by metal-oxide tunnel junctions. The MOSFET-based SE turnstile is a promising device that can accurately transfer SEs at high speed even at room temperature [9] [10] [11]. It consists of a source terminal, a drain terminal, an input gate voltage terminal, a bias voltage terminal and two clock terminals [8].

An accurate transfer with an error rate of 10^{-8} has been achieved by using a seven-tunnel junction pump, however the operating frequency of a SE turnstile is still limited to the order of MHz due to the resistance of the tunnel junctions. [12] has reported an operating frequency of 166MHz. Although the operating frequency is still limited, modulated tunnel barriers have been proposed to improve performance as well as fabrication. Unless explicitly specified, an operating frequency of 166MHz is assumed hereafter in this manuscript.

B. Single-electron Multiple-valued Memories

Single-electron multiple-valued memories (SEMVs) have been proposed [13] for applications in which a novel simulated annealing algorithm (SAA) is utilized to design a single-electron circuit (using a MOSFET-based single-electron turnstile as basic element). The SAA circuit is made of a voltage-controlled single-electron random number generator and the SEMVs with the design objectives of reducing power dissipation and interconnect delay. SAA finds solutions to exponential time complexity (NP-hard) problems, such as the Travel-Salesman-Problem (TSP). SAA is often realized in software, thus limiting a real-time application. Hence, its hardware realization is complex due to the large size of the solution space for the variation operations and the random number range.

The complex arithmetic operations required by this implementation are accomplished using the discrete charge nature of the SE transfer process; so, the SEMVs are used for achieving a sufficiently large storage for the voltage-controlled random number generator (RNG). The SAA circuit is compactly built by using the SEMVs as memory, logic processing unit and RNG. As the logic level of the SEMVs can be accurately modified, the function required for the change in variables can be implemented in the SAA. The SEMVs can be used to store multiple bits and complete the add/subtract operations. It also has the capability to be a voltage-controlled RNG due to the stochastic nature of the single-electron transfer. Randomness is accomplished as follows; by setting the gate voltage V_G to a higher (lower) value, the output bit of the binary stream has a large probability to be "1" ("0"). A transfer speed as high as 100MHz is reported [13]. In the circuit of the SEMVs, a MOSFET-based electrometer has been used for the read operation. When the transistors are turned on, the difference in current represents the number of electrons stored in the storage node (SN). Therefore, the advantage of using the electrometer is that only one MOSFET is used per memory cell at a relatively low power dissipation and small fabrication area in the circuit layout. This circuit element will be assessed in more detail by simulation in a later section.

C. SET/MOS Hybrid Circuit

In this paper, a SET/MOS hybrid circuit is used to sense (measure) the presence of a SE in the memory cell. This is required during the read operation of the memory cell; the diagram of the SET/MOS hybrid circuit is shown in Fig. 1. Its input node is connected to the SN and its output is controlled by the Switch-FET. The circuit proposed in this paper consists of a dual gate (input gate and phase-control gate) SE transistor (SET), a PMOS transistor (as a constant current source) and a NMOS transistor (as a cascade device). The circuit has a control voltage terminal V_{ctrl}, a bias voltage V_{gg}, a phase-control voltage V_{pg} and a power supply V_{dd}.

The SET transistor is a single-electron tunneling device whose operation follows the so-called orthodox theory of single-electronics [12]. Due to the high charging energy resulting from the small total capacitance around the island, the spontaneous junction tunneling is prohibited and the number of electrons in the island becomes discrete under the control of the gate voltage. Therefore, the drain current changes periodically with respect to the gate voltage, showing valleys and peaks

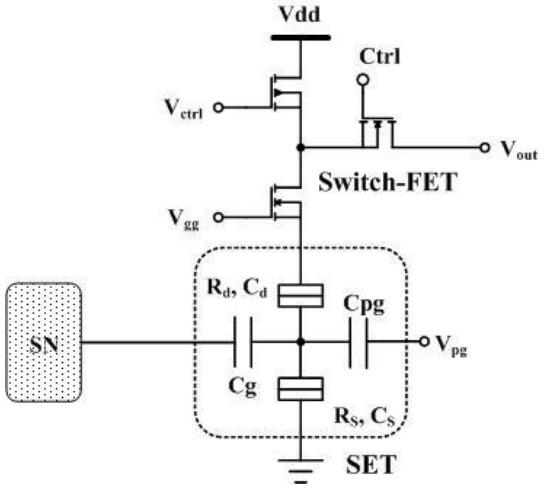

Fig. 1. Schematic diagram of the SET/MOS hybrid circuit.

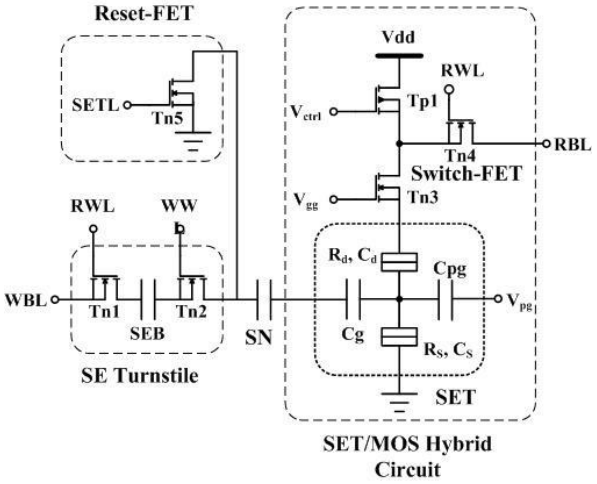

Fig. 2. Proposed hybrid SRAM using a MOSFET-based SE turnstile.

respectively at integer and half-integer numbers of electrons in the island.

As the SET and the NMOS transistor are connected in series in Fig. 1, this unit is referred to as the *serial delay unit*. In this paper, the tunneling resistances (R_d, R_S) and capacitances (C_d, C_S) on the drain and source sides of the SET are equal [11]. The structure of the serial delay unit was initially proposed in [11] [16]. The experimental results show that this circuit can perform as a universal gate; in the SRAM circuit for this application, the parameters of the device are specified differently to perform as *an inverter*. The PMOS transistor in the serial delay unit usually operates in its saturation region as a constant current (CC) source. The output current is controlled by its gate voltage V_{ctrl}. The NMOS transistor with a fixed gate voltage V_{gg} is used to keep the SET drain voltage approximately constant and to generate a large output.

This circuit is utilized for designing a memory cell. The SET transistor has two gates: an input gate and a phase control gate. The input gate receives the output voltage signal from the SN in which the electrons are stored. The received signal induces a Coulomb oscillation of the drain-source current of the SET transistor. The phase control gate (V_{pg}) is used to adjust the inverting characteristic, but it is generally connected to ground.

The operating principles of the serial delay unit are specified as follows. The output current I_o of the PMOS transistor is set at mid-point between the peak and bottom values of the Coulomb oscillating drain-source current I_{dsSET} of the SET. When the number of single-electrons in SN is small, the output voltage signal from SN is low, so the output voltage of the serial delay unit is high, because the inverting SET operates in the nearly cut-off region and the drain-source current of the SET is also low. When the output voltage signal from the SN gradually increases and I_{dsSET} increases to a value higher than I_o, then the output voltage sharply switches to a low value.

Therefore, the proposed hybrid circuit has three advantages over the SEMVs of [13]: (1) combined with the MOS transistors, the hybrid circuit, (especially the SET transistor) can detect the amount of charge in the SE level with a load capability; (2) due to the small gate capacitance of the SET (that electrically couples the SET to the SN), the total amount of transferred charge during operation is significantly smaller than for conventional CMOS devices; (3) by controlling the voltage (V_{ctrl}) of the PMOS, the hybrid circuit can supply a relatively stable output signal to the memory during a read operation, i.e. to the Read Bit Line (RBL).

III. Proposed Memory Cell

The circuit diagram of the proposed SRAM cell is shown in Fig. 2; it consists of a SE turnstile, a SET/MOS hybrid circuit (as a charge-voltage converter), a storage node (SN), a reset MOSFET. The Read Word Line (RWL) and Write Word Line (WWL) are used for the two basic operations of the cell. The Set Line (SETL) is used to reset the stored charge (number of SEs) in the SN. The Write Bit Line (WBL) is the input node and the Read Bit Line (RBL) is the output node of the cell. A single electron is initially assumed in the transfer process. The following operational cycles are analyzed with respect to the simulation result of the proposed memory cell using the parameters in Table I at 45 nm feature size (as in Fig. 3).

1) When RWL is "0", independently of the value of RBL, no read operation is performed in the SRAM. The cell is said to be in a standby state.
2) The "reset" operation is achieved by turning on the reset-FET (Tn5) and Tn2. For example, when the Write Word Line (WWL) and the Reset Line (SETL) are "1" simultaneously, Tn2 and Tn5 are both turned on at the same time. All electrons stored in the single-electron box (SEB) and SN flow to ground, i.e. the memory cell is reset to "0".
3) The "write" operation occurs in Cycle 2; initially, the Write Bit Line (WBL) is "0" when the Read Word Line (RWL) is "1" (to turn the transistor Tn1 on). However, as the information to be written is "0", then there is no electron to be transferred into the single-electron box (SEB). Subsequently in Cycle 2, WWL is "1" and RWL is "0"; therefore, Tn1 is turned off and Tn2 is turned on. So, a "0" is written into the SN, i.e. there is no voltage change in the RBL.
4) The Read "0" operation occurs at Cycle 3. Following Cycle 2, the information (i.e. "0") is in the SN; the charge-voltage

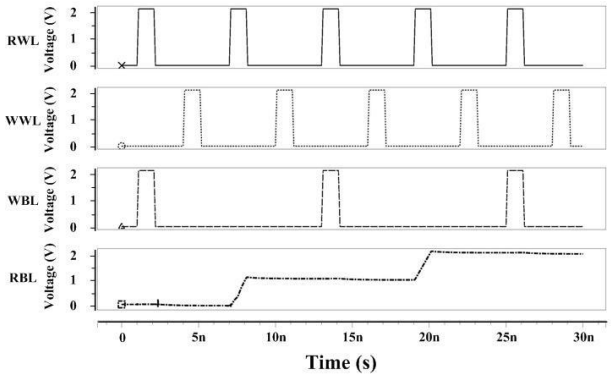

Fig. 3. HSPICE timing diagram of proposed SRAM cell at 45nm node.

converter (consisting of Tn3, Tp1 and SET1) converts the stored electron into the corresponding voltage. As the SN has a "0", there is no electron in SN. In Cycle 3, RWL is "1" so transistor Tn4 is turned on. The "0" will be then read through the Read Bit Line (RBL).

5) The Write "1" operation is given follows. In Cycle 1, RWL and WBL are "1" simultaneously, (turning on the transistor Tn1). In this cycle, as WBL is "1", a single electron is transferred into the SEB. Following this event, WWL is "1", the Tn1 is turned off in this cycle. Moreover, Tn2 is turned on when RWL is "0". In this process, the SE is transferred into the SN, i.e. the write "1" operation takes place.
6) The process to read a "1" is as follows. As a "1" is stored in the memory, then there is a single electron stored in the SN. The converter of the SET/MOS hybrid circuit will sense the stored SE in the SN by converting it into a high voltage level for Tn4 to be on. In Cycle 2, RWL is "1" and Tn4 is turned on. So, the "1" is read and a voltage change occurs as observed through the RBL.

IV. Simulation of Memory Cell

The proposed SRAM cell has been simulated using HSPICE by combining the models of its different elements (such as the SET/MOS hybrid circuit and the MOSFET-based SE turnstile) [7] [8] as described in a previous section.

For simulating single-electron devices, few tools are available as reported in the technical literature. Notable among these are SIMON [17] and MOSES [18]. However, these simulation tools cannot include many electronic components such as diodes and transistors. So the SET circuit elements have been simulated by HSPICE models. These models are either phenomenological in nature, or simplification of the orthodox theory of single-electron tunneling, or specifically tailored extensions of HSPICE. The compact SPICE model to describe the behavior of the SET based on Lientschnig's SET [7] has been used in this paper; its accuracy has been verified by both the Monte Carlo simulator SIMON [17] and experimental results [19].

For simulating the operation of the SE turnstile, [8] has presented a novel HSPICE circuit model applicable at nanometric feature sizes. This SE model is used in this paper and consists of two nearly similar parts whose operation is independent of each other; this feature permits to accurately model the sequential transfer of electrons through the turnstile as a change of voltage in the storage node. It therefore avoids the transient (current-based) nature of a previous model. The model has been simulated and results have shown that it can correctly operate at 32 and 45 nm with high stability in its operation [8]. With the circuit architecture and functions discussed previously, the SE turnstile model of [8] has been slightly modified to change the voltage levels to negative values. This is required because they correspond to the charges of the SEs and the SET/MOS hybrid circuit operates as an inverter. It can read the SE(s) stored in the SN and its output voltage levels correspond to the number of electrons stored in the SN.

TABLE I
Device Parameters for HSPICE Simulation

Index	Parameter		Value
Feature Size		45 nm	32 nm
Temperature		300 K	300 K
Power Supply	Vdd	2.1 V	0.9 V
	-Vdd	-2.1 V	-0.9 V
SE turnstile	W_{FET1}, W_{FET2}	45 nm	32 nm
	L_{FET1}, L_{FET2}	45 nm	32 nm
	Vg1, Vg2	2.1 V	0.9 V
	V_h	2.1 V	0.9 V
	V_l	-2.1 V	-0.9 V
	C_{SEB}	0.5 aF	0.5 aF
	C_{SN}	10 aF	10 aF
SET	C_S, C_d	0.2 aF	0.2 aF
	CgSET	0.4 aF	0.4 aF
	CpgSET	0.1 aF	0.1 aF
	R_S, R_d	100 KΩ	100 KΩ
	V_{pg}	0 V	0 V
Hybrid Circuit	V_{ctrl}	-2.1 V	-0.9 V
	V_{gg}	2.1 V	0.9 V

Table I lists the device-level simulation parameters and the values used in the HSPICE simulation of the proposed memory cell. MOS transistors with 45 and 32 nm feature sizes are used. Fig. 3 shows the obtained timing diagrams of the proposed SRAM cell at 45 nm. As discussed previously for the function of the SET/MOS hybrid circuit, simulation has shown that the voltage swings can be controlled accurately by V_{gg}, while V_{ctrl} is utilized to modify the output current of RBL.

The simulation plots show that the voltage can be gradually increased when RWL and WBL are both "1". Then with WWL set to "1", the single-electron stored in the SEB is transferred into the SN. This process means that the "1" is written in the SN. Each pulse at the input source node can transfer a SE when RWL and WWL are path on. So the increased voltage levels only appear at this time. Finally for both simulated cases and by taking into account the transfer error rate of the SE turnstile [20], the frequency of operation for the SRAM cell is given by 166MHz [20].

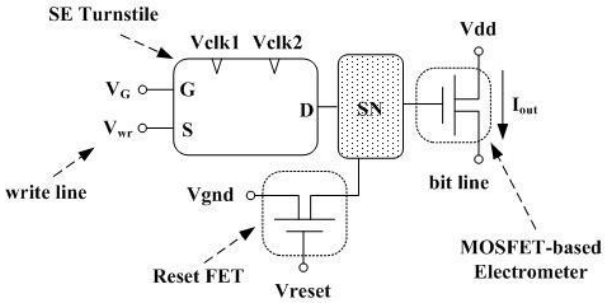

Fig. 4. Schematic diagram of the single-electron multiple-valued memory (SEMV) circuit [13].

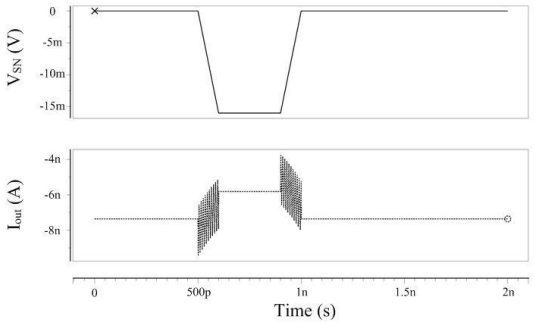

Fig. 5. Simulation of MOSFET-based electrometer at 32nm node.

V. Performance Evaluation of Circuit Elements

In this section, a detailed evaluation of different circuit elements (and related performance features) of the proposed memory cell is pursued using simulation by HSPICE.

A. SET/MOS Hybrid Circuit Evaluation

1) Read Operation

A detailed comparison of two possible implementations of a circuit element and related mechanisms (the SET/MOS hybrid circuit and the MOSFET-based electrometer [13]) for the read operation is presented. For simulation, a negative voltage pulse is imposed on the Storage Node (SN) to represent the stored (transferred) single electron at 32 nm feature size and 166 MHz operating frequency. Table II shows all other simulation parameters for comparing the read mechanism.

Consider first the MOSFET-based electrometer [13] of Fig. 4; the simulation results for the read operation are shown in Fig. 5. When a voltage pulse is provided at the input node (the SN), the current through the MOSFET shows a ringing behavior in the transitions (in a scale of nA) of the output current. This can be explained as follows. There are three operational modes for an n-channel MOSFET. When $V_{GS}<V_{th}$ (where V_{th} is the threshold voltage), the transistor is turned off and there is no conduction between drain and source. As per the basic threshold model, the transistor is working in the cutoff mode, so the current between drain and source should ideally be zero (as the transistor is a turned-off switch). However, there is a weak-inversion current (sometimes also referred to as the subthreshold leakage) due to the presence of a Boltzmann distribution of electron energies. This phenomenon leads to some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current. This current has an exponential function of the gate–source voltage. In the weak inversion mode, the current varies exponentially with the gate-to-source bias V_{GS}; this is approximately given by [22]:

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}} \quad (1)$$

where I_{D0} is the current at $V_{GS}=V_{th}$. The slope factor n is given by

$$n = 1 + \frac{C_D}{C_{OX}} \quad (2)$$

where C_D is the capacitance of the depletion layer and C_{OX} is the capacitance of the oxide layer. Therefore, although $V_{GS}<V_{th}$ and the transistor in the MOSFET-based electrometer works in the cutoff mode, the variation of V_{GS} causes a change in the drain current (I_D). This effect is shown in Fig. 6 by the ringing behavior for the transitions to represent the electron transfer event.

At the beginning of the up-transition, the current changes severely and many pulses appear prior to reaching a stable level. Furthermore, this ringing phenomenon occurs also during the second (downward) transition; these current variations have small values (in the nA range), but they can be still detected. The read operation is effectively achieved by turning on and sensing the current of the MOSFET-based electrometer in the SEMV of Fig. 4, so the output current for the read operation is affected (Fig. 5). The electrometer is capacitively coupled to the SN, and its current changes discretely with the number of electrons in the storage node [21].

Fig. 6 shows the simulation results for the read operation in the proposed SET/MOS hybrid circuit. As shown previously by simulation, the SN has been directly provided with an input voltage signal; furthermore, the Switch-FET has been kept on to mitigate its effect on the output signal. As shown in Fig. 6, the output is stable in signal variation once a voltage change occurs at the input. This is significantly better than for the

TABLE II
Device Parameters for HSPICE Simulation, Read Operation Comparison

Index	Parameter	Value
Feature Size		32 nm
Temperature		300 K
Power Supply	Vdd	0.9 V
	-Vdd	-0.9 V
SET	C_S, C_d	0.2 aF
	CgSET	0.4 aF
	CpgSET	0.1 aF
	R_S, R_d	100 KΩ
	Vpg	0 V
Hybrid Circuit	V_{ctrl}	-0.9 V
	V_{gg}	0.9 V
MOSFET-based Electrometer	W_{FET}	32 nm
	L_{FET}	32 nm

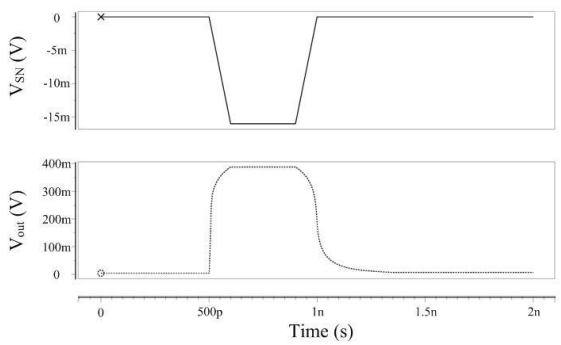

Fig. 6. Simulation of SET/MOS hybrid circuit at 32nm node.

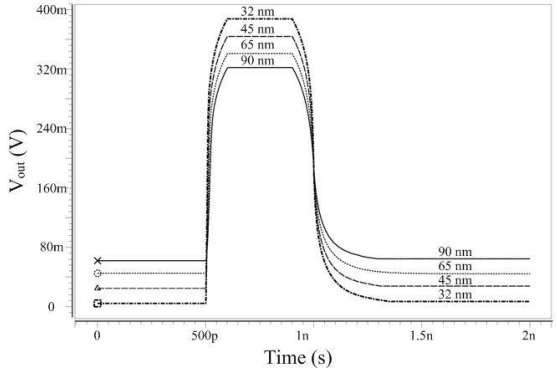

Fig. 7. V_{out} of the SET/MOS hybrid circuit vs time by varying MOSFET feature size.

MOSFET-based electrometer, thus detecting the state of the SN and the presence of an electron on a voltage-basis. The stable high value of the output voltage signal in Fig. 6 shows that the hybrid circuit can monitor the stored (transferred) electrons, i.e. for the read operation, the circuit can correctly sense the negative voltage signal and change it into a positive value (as final output).

These two circuits (Fig. 1 and 4) have totally different mechanisms for the same output sensing function. In addition to the ringing behavior, the MOSFET-based electrometer of [13] has an output current variation that is relatively small to monitor. The proposed hybrid circuit has a rather sharp voltage signal that is compatible with digital circuit operation. Moreover, memory operations will benefit from a voltage level signal, thus avoiding the severe change in output current experienced by [13] and the likely damage due to stress in the sensing circuit. Therefore, simulation has confirmed that for a SE based operation, the proposed SET/MOS hybrid circuit offers substantial advantages compared with [13] and its use is viable for the memory operations of the proposed cell.

2) MOSFETs

The proposed SET/MOS hybrid circuit is used to sense and measure the number of SEs stored in the memory cell. The circuit performs as an universal gate in which the PMOS and NMOS transistors have specific functions. The PMOS transistor is used as a constant current source by operating in the saturation region; the NMOS transistor generates a large output by applying an appropriate voltage value V_{gg}. Next, the output voltage signal will be assessed by scaling the MOSFET feature size.

The simulation results for V_{out} are shown in Fig. 7 (also in this case, the same input signal as in Fig. 6 has been utilized); the feature size of the MOSFETs (both the PMOS and the NMOS transistors) has been varied from 90 to 32 nm. A lower feature size leads to a relatively higher sensitivity of the hybrid circuit, i.e. the output signal at 90 nm is 320 mV, while at 32nm it is 400mV. Moreover, the output voltage signal at lower feature sizes shows a larger range as reflected by the difference between low and high voltage values. The larger range also confirms that the hybrid circuit is more sensitive at lower feature sizes, thus providing an additional positive feature in the design of the memory cell.

3) SET Transistor

The SET transistor is an important element of the proposed SET/MOS hybrid circuit; it is used to sense the electrons stored in the SN and convert the output signal to a voltage level (as corresponding to the number of stored electrons). Similar to the SE turnstile [8], the SET is formed by the tunneling junctions originating from the phenomenon of Coulomb blockade (CB). This is advantageous for designing memory cells with low power consumption and large electrical margins, because it is possible to control the transfer of individual electrons at extremely small statistical fluctuations (even with small device dimensions) [24]. So, the internal parameters of the SET are very important for performance and robustness of the proposed memory cell.

Fig. 8 shows the simulation results for the output voltage V_{out} by varying the tunnel resistance R_T at C_j = 1aF. This affects the formation of the CB in the SET transistors. If the tunnel barriers are at least insufficiently opaque, then either an island will likely not be charged or electrons will not be localized (such as on a quantum dot), because there will be no constraint on an electron to be confined within a specific location. Qualitatively, consider an electron transfer based on CB at a single tunnel barrier [25]; to avoid thermally activated electron transfers, the thermal energy k_BT must be lower than the charging energy (denoted by E_C), i.e.

$$k_B T < E_C = \frac{e^2}{C_j} \tag{3}$$

where C_j is the charge capacitance in a single junction and applicable also to C_S and C_d in the hybrid circuit. The tunnel resistance R_T must also be sufficiently large to allow individual electrons to tunnel through the barrier, provided events do not overlap. Hence, the time Δt between two successive events must be larger than the time duration τ of a single tunnel event. Δt allows for charge fluctuations to occur and is given by

$$\Delta t \approx R_T C_j \approx \frac{eR_T}{V} \tag{4}$$

where V is the tunnel junction biased voltage. Furthermore, the time duration τ is given by the following equation

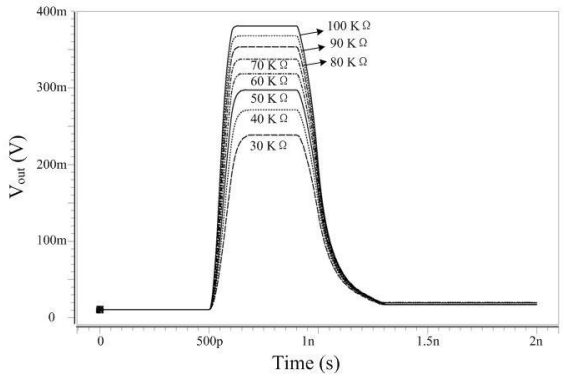

Fig. 8. V_{out} of the SET/MOS hybrid circuit vs time by varying Tunnel Resistance R_T at 32 nm.

$$\tau = \frac{\hbar}{eV} \tag{5}$$

By combining (4) and (5), the tunnel resistance is given by

$$R_T >> \frac{\hbar}{e^2} = 25813\,\Omega \tag{6}$$

As per the above analysis, the value of R_T has been varied during simulation from 20 k Ω to 100 k Ω to allow for a comprehensive evaluation of its influence on the output signal.

As shown in Fig. 8, the range of the output voltage is affected by the variation of the tunnel resistance R_T; with a decrease of the resistance, the high output level decreases significantly till the functionality of the hybrid circuit is completely lost, thus confirming the limit set by (6). Combined with the variation of the tunnel resistance R_T, Fig. 9 shows the results by varying the capacitance C_j for correct functionality of the proposed hybrid circuit, i.e. C_j is changed to ensure circuit operation under different values of R_T, as in (4). Fig. 9 shows the boundary plots for the region of correct operation under feature sizes of 32 and 45 nm; so for example as reported previously, the values of 1aF and 100 k Ω generate an acceptable output signal in the proposed hybrid circuit. Compared with 32 nm, a feature size of 45 nm results in a lower value of the duration time τ, thus requiring a relatively smaller value for the product of (4), i.e. the hybrid circuit at 32 nm feature size has a more severe requirement in the capacitance and resistance values.

VI. Performance Evaluation of Memory Cell

In this section, different aspects related to the assessment of the proposed memory cell are investigated in detail; its circuit-level performance is pursued.

A. Circuit Performance

Performance evaluation and related metrics will be presented and discussed initially at circuit level. Table III shows the figures of merit for the proposed SRAM cell as simulated using HSPICE at the two different feature sizes of 45 and 32 nm. The number of electrons transferred by the SE turnstile (N) depends on the value of Cg, i.e. the capacitance between the gates and the SEB. In this paper, it is assumed that $Cg/C_0=N$, where C_0=1 aF as a unit capacitance. So, the voltage level can be controlled by utilizing different values of the capacitance Cg. In this case, the capacitance of the SE turnstile model has been set to C_0, i.e. the number of transferred electrons is one per cycle.

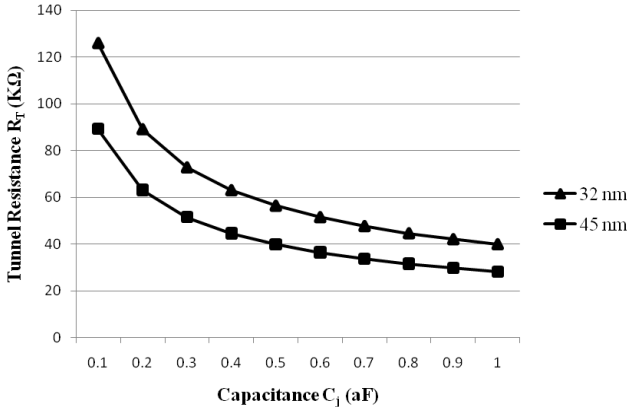

Fig. 9. Tunnel Resistance R_T (Rs, Rd) vs Capacitance C_j (Cs, Cd) for SET/MOS hybrid circuit at 32 and 45 nm.

1) Average Write/Read Delay

Consider the delay for the two basic memory operations, as reported in Table III; both delays are reduced as the feature size decreases for the MOSFETs. However, this is related to the operating frequency of the proposed SRAM cell by two limiting factors. The first limiting factor is given by the transfer error rate of the SE turnstile. The "write" operation is accomplished through the SE turnstile, so its operating frequency has a significant effect on the write delay. The transfer accuracy deteriorates if the falling time t_{fall} of the clock signal is too small [20]; hence, the write delay of the proposed SRAM cell is higher than the read delay. Furthermore, the mechanism of the "write" operation in the proposed memory cell is different from a conventional (CMOS-based) SRAM. In the proposed cell, once an operational cycle is completed, a pulse must be generated to turn on Tn5 (SET-FET) to reset the SN back to "0". So, there is no significant and direct improvement in delay for the write operation of "0"; the write delay is mostly affected by the SE transfer speed, not the characteristics of the MOSFET (as occurring in a conventional memory circuit).

The relative slow speed of a SE-based memory design avoids a transfer error in charge-state circuits. For a MOSFET-based turnstile, it can be categorized into thermal and dynamic errors; at a lower operating speed, thermal errors dominate and dynamic errors can be neglected [21]. This failure mode is inherent to the SE transfer process and can be only mitigated

TABLE III
HSPICE Simulation Results for SRAM Cell

Feature Size	45 nm	32 nm
Temperature (K)	300 K	300 K
Average Write Delay (ns)	9.04 ns	8.73 ns
Average Read Delay (ns)	3.06 ns	2.96 ns
Vdd (V)	2.1 V	0.9 V
Average Power Dissipation (W)	1.38E-6 W	1.27E-6 W
Leakage Current (A)	1.27E-6 A	5.25E-7 A

using a suitable frequency. As discussed in [21], the operating frequency is usually set to 166MHz.

The second limiting factor is the delay incurred in the SET/MOS hybrid circuit (as charge-voltage converter) for the read operation. As the SET can sense the number of SEs stored in the SN, the circuit converts them into a voltage level; a portion of the read delay is related to the high reactive response of the SET. The simulation result shows that the read delay td is around 3 ns. In the worst case, the delay of the SET/MOS hybrid circuit is given by $td=C_{tot}V_o/I_o$, where t_d is the delay time, C_{tot} is the total load and inherent capacitance and I_o is the bias current. As the proposed SRAM require two repulsive clock signals, the maximum operating frequency is $f_{max}=1/2\ t_d$, which is approximately 150 MHz using the parameters of Table I.

2) Power Dissipation

The power dissipation of the proposed SRAM cell is very low, because most of its operations are achieved by transferring SEs. In theory, the power dissipation is given by $W=N_{tot}eV_{SS}f$, where, N_{tot} is the total number of electrons transferred by the SE turnstile in one operating cycle, e is the electron charge and f is the operating frequency. Simulation results show that the average power dissipation (that may include leakage and repulsive clock components) is around 1300 nW, slightly decreasing with feature size. This is expected because the SE turnstile has very small power consumption and most of its power is used to transfer each single electron. Also, the total power dissipation of the proposed SRAM is mostly due to the SET/MOS hybrid circuit; in addition to a SET transistor, there are only three transistors. Tn3 and Tp1 stabilize the output current and modify the output voltage swing. The results of Table III include power dissipation due to leakage as well as the power dissipated by the electronic components of the HSPICE model of the SE turnstile [8] too, hence larger than expected values. Also as the proposed SRAM cell requires two repulsive clock signals, it is anticipated that extra power will be dissipated by them as determined by the interconnect, gate capacitances and frequency [13]. However, its value is smaller than the power dissipation of the SET/MOS hybrid circuit, but larger than the SE turnstile. The reduction in power dissipation is further accomplished by scaling the feature size from 45 to 32 nm, showing only a modest improvement in this figure of merit.

3) Leakage Current

The results show that the leakage currents are in the range of 0.5 μA to 1.5 μA. These results follow from the utilization of the SE transfer mechanism in the proposed cell. The SE transfer process effectively replaces the conventional write mechanism, thus it may also lead to a relatively large decrease of the active leakage component. Hence, the leakage current of the proposed SRAM occurs mostly in the standby mode of the SET/MOS hybrid circuit. Due to the biasing voltages (V_{dd}, V_{gg} and V_{ctrl}), there exists a transistor path in the circuit from the power supply to ground, even when there is no input signal. Along this path, Tn3 and Tp1 are turned on during each operation. The use of the PMOS Tp1 is to generate a stable current to the output node. So when the SRAM is in standby, this leakage current cannot be mitigated.

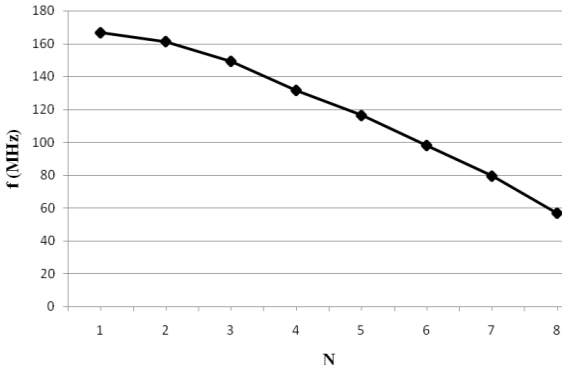

Fig. 10. Operating Frequency vs number of simultaneously transferred electrons at 32nm node.

B. Electron Transfer Characteristics

In the previous discussion for the evaluation of the proposed memory cell, the number of transferred electrons (N) has always been assumed to be 1; however, the SE turnstile can be used to transfer any number of electrons. This permits to design memory cells with multi-value information; as one of the fundamental elements of the proposed memory cell, the SE turnstile allows a precise transfer of electrons, while still retaining a stable output signal. Next, two cases of electron transfer are considered; the simultaneous and the sequential transfers of electrons are assessed to show the frequency characteristics of the proposed memory cell.

1) Simultaneous Transfer

Previous sections have shown that the capacitance between the gates and the SEB affects the number of electrons that are transferred in each cycle. So, the operating frequency of the proposed memory cell depends on the simultaneous transfer of electrons (whose number is given by N). Fig. 10 shows the operating frequency of the memory cell versus N (for a range of N from 1 to 8) at $V_B=0$ and 32nm. For example when N=2, the number of electrons transferred by the SE turnstile is two, i.e. in each transfer cycle, two electrons are simultaneously transferred through the SEB into the SN and read by the hybrid circuit. This behavior has already been demonstrated previously by the change of voltage levels in the simulation results; so, with an increase in the capacitance Cg, the voltage levels confirm the electron transfer events, including the write and read operations.

However, as result of the characteristics of the SE turnstile and the HSPICE simulation models that have been utilized [7] [8] for the voltage-controlled current sources (as comparators), the operating frequency is affected by N and therefore, it has to be modified for stability of the output. In the previous simulation results, an operating frequency of 166 MHz has been used for N=1; by increasing N, the simulation of the proposed memory cell at 32 nm node requires a lower operating frequency to preserve the integrity of the output signal. The simulation results of Fig. 10 show an almost (inverse) linear trend with respect to N, i.e. a lower operating frequency is accounted by

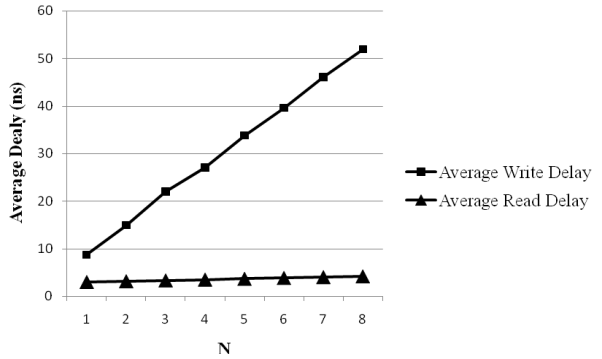

Fig. 11. Average Delay vs N for sequential electron transfer at 32nm node.

increasing N. The output voltage changes to a higher value with an increase of N, also resulting in additional time for the "write" operations by the SE turnstile. Also, more time is needed for the sensing operation by the SET/MOS hybrid circuit, while the electrons are transferred into the SN.

2) Sequential Transfer

Previously the simulation results for a simultaneous transfer were presented; in this section, electrons are sequentially transferred in the proposed memory cell, i.e. one by one till the desired value of N is reached. This process requires multiple "write" operations, the memory cell senses the stored electrons only once per cycle since the electron transfer occurs one by one (thus also incurring in a different read time as related to the value of N). The simulation results are shown in Fig. 11.

In this figure, the average write delay shows a sharp linear increase as function of N due to the sequential nature of this process. It is evident that the time interval of the sequential electron transfer is significantly limited by the operating frequency of the SE turnstile; this leads to an incremental increase of the average write delay. Compared to the sharp variation for the average write delay, the average read delay is rather limited showing only a small increase versus N. The read operation of the proposed memory cell is accomplished by the SET/MOS hybrid circuit; due to the highly sensitive SET transistor, the stored electrons in the SN can be counted and efficiently converted to a voltage level. The small increase of this operation is mainly due to the change in voltage level, because a larger number of stored electrons imply an increase in voltage, translating into a longer time delay for the read operation.

C. Area

The proposed memory consists of the SE turnstile and the SET/MOS hybrid circuit as experimentally demonstrated and fabricated in [24]. [24] has shown that the turnstile and the coupling SET (so exclusive of the three MOSFETs of the hybrid circuit and the Reset-FET Tn5) can be patterned on a 30 nm thick silicon-on-insulator layer using pattern-dependent-oxidation (PADOX) [24]. By considering requirements such as gate length, spacing between Tn1 and Tn2 and the transistors in the hybrid and reset circuits, the total area of the proposed memory cell is approximately 850 λ^2. A conventional CMOS (6T) SRAM has an area of 1092 λ^2 [27]; so, the proposed memory cell requires less area, hence accomplishing a higher density in integration.

D. Static Noise Margin

The so-called Static Noise Margin (SNM) must be considered for assessing the stability and robustness of a memory cell. The SNM is defined based on the input to output voltage characteristics (VTC) [28] to characterize the robustness to noise. As the proposed cell utilizes the basic mechanism of electron transfer using single-electron devices, each memory operation must be treated separately.

Consider first the "write" operation using the SE turnstile, whose operation is dependent on the control gates for RWL and WWL. Different from a conventional 6T SRAM, the proposed memory transfers electrons following the application of sequential pulses on RWL and WWL. The electrons stored in SEB and SN are represented by voltage levels, not a continuous voltage variation of a charging/discharging process. The simulation results of the SE turnstile with both RWL and WWL at a high voltage level are generated using the parameters listed in Table I at 32 nm feature size; the measured values are 0.409V for V_L and 0.611V for V_H under a binary memory write operation at a curve slope of -1. So, the Static Noise Margin Low (SNM_L) and Static Noise Margin High (SNM_H) for the write operation are 0.409V and 0.289V, respectively, i.e. by subtracting 0V from V_L and V_H from Vdd (i.e. 0.9V) [28]. Compared with 0.390V as the SNM_L for a conventional 6T CMOS SRAM [29], the proposed cell has a larger noise margin, thus making it more stable for a write operation.

Consider next the "read" operation; this is mainly related on the SET/MOS hybrid circuit. As per the evaluation in a previous section, its transfer characteristics have been simulated using the parameter listed in Table I at 32 nm feature size. In the simulation, RWL is set to a constant high voltage level and the SET transistor is characterized for the inverting property. In this case, the measured values of V_L and V_H for the read operation are 0.158V and 0.479V, respectively; hence, the SNM_L and SNM_H are 0.158V and 0.421V. As a 6T CMOS SRAM has a SNM_L 0.16V [30], there is an almost negligible penalty in the read static noise margin.

VII. Ternary CAM Cell Design

In this section the hybrid design of an SRAM cell proposed in previous sections is extended to a TCAM. The basic principle of the proposed memory is to replace a conventional CMOS-based SRAM cell by a SET-based static memory cell with a SET/MOS circuit. In the simplest case, this requires the SET-based design to have the following functions. (1) A ternary level data storage function implemented by the SET-based memory cell. (2) A data matching function utilizing the multi-peak periodic drain-current characteristics of a SET with dynamic phase-shift control.

However, changes are required in the design. The biasing voltage imposed on the control gate of a SET transistor in a SET/MOS circuit must be selected appropriately, as it may lead

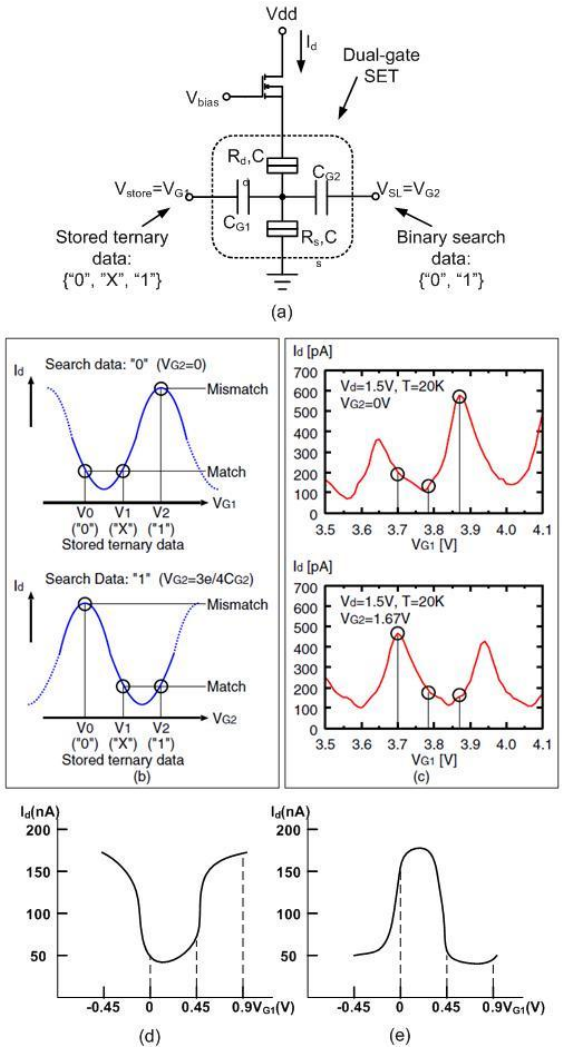

Fig. 12. Operation principles of ternary matching: (a) matching circuit consisting of a dual-gate SET and a cascode MOSFET, (b) ternary matching and (c) measured drain current characteristics [8], (d) and (e) simulated drain current characteristics at V_{G1}=0V, V_{G1}=0.9V, respectively (at 32nm).

to totally different I-V characteristics. Also, the arrangement of the Word Line (WL) and the Bit Line (BL) must be changed because a cell using SET-based devices needs two WLs and BLs for the "read" and "write" operations and must accommodate ternary matching too. Thus, a novel circuit for the cell is required.

Fig. 12 (a) shows the matching circuit consisting of a dual-gate SET with a cascode MOSFET, in which V_{G1} accepts the stored ternary data and V_{G2} accepts the searched binary data. For the matching operation, V_{G2} is used to shift the periodic drain-current characteristics of the dual-gate SET, as illustrated in Fig. 12 (b) [14]. Initially the following cases are considered. (1) Assume V_{G2}=0, i.e. the searched data is "0"; so, the SET is turned ON only when $V_{G1}=V_2$ (the stored data is "1"). When this condition is met, the drain current through the matching SET causes a high voltage with a discharge of the ML. Hence, ML is low indicating a "Mismatch". (2) When V_{G1} is either "0" or "X", the matching SET is not turned ON; so, ML is always high with no discharge process. So, both of these two conditions show the "Match" result.

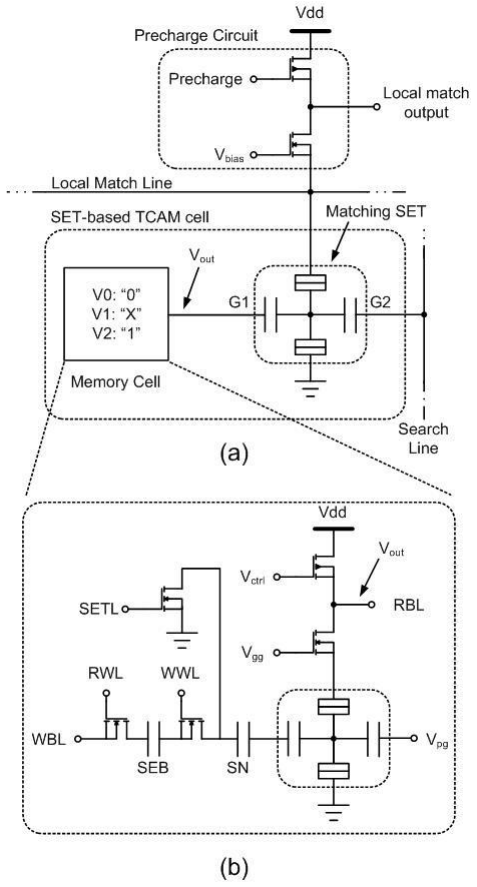

Fig. 13. Proposed TCAM cell and precharge circuit: (a) Cell structure and precharge circuit (b) SET-based memory cell.

Assume $V_{G2}=3e/4C_{G2}$ (Here, $e=1.602\times10^{-19}$ Coulombs); the phase is shifted left by 3/4 of the period. The following two cases are possible. (A) As the searched data is "1", then based on the I-V characteristics, the SET is turned ON only when $V_{G1}=V_0$ (the stored data is "0"). This operation is similar to the condition of "Mismatch". (B) When V_{G1} is either "X" or "1", the matching SET is not turned ON, so both showing the "Match" result. Fig. 12 (c) shows the measured characteristics of the fabricated dual-gate SET of [14] and demonstrates the capabilities of the TCAM cell using this technique. In a previous paper [15], this characteristic has been successfully employed to perform an XOR logic function. Next it is utilized for implementing the comparison function in a TCAM cell also based on SET. Fig. 12 (d) and (e) show the simulation results using the SET model in [7] and the parameters in Table I confirming the correctness of the drain current characteristics.

Fig. 13 (a) shows the proposed TCAM cell structure using SETs and the precharge circuit. The structure of the SET-based TCAM consists of a memory cell, a Local Match Line (LML), a Search Line (SL) (note that the Bit Lines (BLs) and Word Lines (WLs) are omitted in Fig. 13 (a)). In the proposed cell, the matching SETs are connected to a LML, such that LML can be connected to only a number of matching SETs (for a low LML capacitance). Furthermore, several TCAM cells can share the precharge circuit as depending on specific performance requirements.

The dual-gate SET in Fig. 13 (a) is used for the data matching operation. It receives the stored data from the output of the memory cell; as the ternary memory using a SE turnstile can be designed with 6 transistors (1 SET and 5 MOSFETs), the total transistor count for the proposed cell is 9. Compared with a traditional CMOS-based TCAM cell that requires two 6-transistor CMOS SRAMs and 4 matching transistors, the number of transistors is reduced by nearly 50%. Fig. 13 (b) illustrates the proposed SET-based memory cell. This circuit consists of a SE turnstile [26], a SET/MOS circuit, a storage node (SN), a reset MOSFET. (A) The Read Word Line (RWL) and Write Word Line (WWL) are used for the two basic operations of the cell. (B) The Set Line (SETL) is used to reset the stored charge (number of SEs) in the SN. (C) The Write Bit Line (WBL) is the input node and the Read Bit Line (RBL) is the output node of the cell. (D) The SN is utilized to store multi-level voltage data.

[26] has already demonstrated the basic operations of a SE turnstile with a memory circuit; in this paper, a SET/CMOS circuit is employed to store the ternary data (i.e. "0", "X" and "1"). Fig. 14 shows the simulation timing diagram of the proposed TCAM cell at 45 nm, using parameters listed in Table IV. The memory cell stores the ternary data ("0", "X" and "1") to be written; the cell is connected to LML by the SET matching circuit. As per previous discussion, if the searched data is "0", only when the stored data is "1", the SET is ON and a "Mismatch" output is generated. If the searched data is "1", then only when the stored data is "0", as a result of the phase-shift characteristic, the SET is turned ON, resulting in a "Mismatch" output. When the stored data is "X", then independently of the searched data, a "Match" output is always generated. When the searched data are equal to the stored data, a "Match" output is generated.

Next, the HSPICE simulation results of the proposed TCAM cell are initially presented. Table IV shows the values of all device parameters as applicable to the simulation of the proposed TCAM cell. As the "write" operation is accomplished through the SE turnstile [26], then the transfer error rate is the most significant limiting factor on its operational frequency; as based on [26], this frequency is set to 166 MHz. Initially, by controlling the SE turnstile, electrons are transferred into the SN; the output voltage levels are converted as "Write data". Using the matching SET, they are compared with the "Searched data" on the searching line. The final output (as outcome) is as expected. By utilizing the phase-shift characteristics of the dual-gate SET, for "X" as stored ternary data, the output always shows a "Match" independently of the "Searched data". Hence through this simulation, the correct write and matching operations of the proposed TCAM cell have been confirmed. The HSPICE device model of [26] [7] is utilized for the SET. Throughout this simulation, the voltages of the ternary signals are initially stored in the memory cell through the write operation; then, the SET/MOS circuit converts them into positive voltage levels at the RBL (V_{out}). The matching operation is performed to generate the local match output.

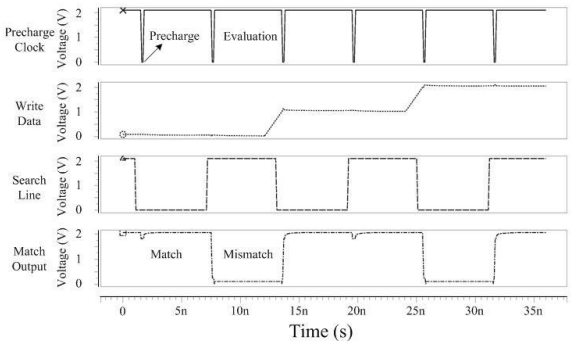

Fig. 14. Simulated results of timing diagram of TCAM at 45 nm.

Based on the simulation parameters presented in Table IV, an extensive analysis of the matching operation is pursued next. The operations and waveforms of the proposed TCAM cell are shown in Fig. 14; these plots are applicable to a single TCAM cell that stores the three logic values ("0", "X" and "1"). By considering the combinations of the two different logic values ("0", "1") in the Searching Line (SL), six matching operations (one per cycle) must be considered as follows.

(1) In the first cycle, no "write" operation is performed in the memory cell and its output of the "Write data" is "0". Compared with the "Search data" in SL, the matching operation is achieved by the matching SET; the "Match" output is high. The cell has a "Match" condition based on the comparison of the same data, i.e. "0".

(2) When the "Search data" is "1" and the "Write data" is still "0", the "Match" output is low (Cycle 2). As previously discussed, in this case, the phase is shifted by a 3/4 of a period;

TABLE IV
DEVICE PARAMETERS FOR HSPICE SIMULATION

Index	Parameter		Value
Feature Size		45 nm	32 nm
Temperature		300 K	300 K
Power Supply	Vdd	2.1 V	0.9 V
	-Vdd	-2.1 V	-0.9 V
SE turnstile	W_{FET1}, W_{FET2}	45 nm	32 nm
	L_{FET1}, L_{FET2}	45 nm	32 nm
	Vg1, Vg2	2.1 V	0.9 V
	V_h	2.1 V	0.9 V
	V_l	-2.1 V	-0.9 V
	C_{SEB}	0.5 aF	0.5 aF
	C_{SN}	10 aF	10 aF
SET in MEM cell	C_S, C_d	0.2 aF	0.2 aF
	CgSET	0.4 aF	0.4 aF
	CpgSET	0.1 aF	0.1 aF
	R_S, R_d	100 KΩ	100 KΩ
	V_{pg}	0 V	0 V
Hybrid Circuit	V_{ctrl}	-2.1 V	-0.9 V
	V_{gg}	2.1 V	0.9 V
Matching SET	C_S, C_d	0.9 aF	0.9 aF
	C_{G1}, C_{G2}	0.05 aF	0.13 aF
	R_S, R_d	100 KΩ	100 KΩ

this results in a high drain current through the matching SET. Hence, LML is discharged; the output is low representing the "Mismatch" outcome.

(3) The "write" operation occurs in Cycle 3; as the information to be written is "X" (a middle voltage level), there is an electron transferred into the Storage Node (SN) of the memory cell. So, "X" is shown in the "Write data" and compared with the data in SL. As the "Searched data" is "0" (Fig. 12(b)), the drain current through the matching SET is low and the "Match" is completed without discharging LML.

(4) As per the phase-shift characteristics of the matching SET and based on the I-V characteristics of the SET, when the "Searched data" is "1", a "Match" will occur at the output (Cycle 4). By utilizing this characteristic (i.e. the phase is shifted by 3/4 of a period), the drain current is low to hold the charge state of the LML. However, there is a small voltage decrease in the output node as result of the precharged clock (CLK) in the ML. Prior to the evaluation in each cycle, ML is precharged again; a CLK pulse causes a temporary decrease that is mitigated in the next evaluation period.

(5) In Cycle 5, the second electron is transferred into the SN, causing a voltage increase of the "Write data" (i.e. to "1"); however, the "Searched data" in SL is "0". Following this event, the matching SET is turned on in this cycle and a high drain current passes through it to discharge the LML. So the "Match" is low indicating a "Mismatch" condition.

(6) Finally, when the "Searched data" is "1" (same as the "Write data"), the matching SET is turned off again (Cycle 6). LML is high following the precharge process in this cycle because the drain current is low. So, a "Match" occurs as observed through the "Match" output.

The above discussion has considered the six combinations of the "Write data" ("0", "X" and "1") and the "Searched data" ("0", "1"). These results show that the proposed TCAM cell works correctly using HSPICE simulation and employs compatible models for all SET devices in the proposed circuit of the memory cell.

The performance evaluation and relevant metrics for assessing a single TCAM cell are presented and discussed in this section. Ahead of them, the influences of SET internal parameters were characterized in [14]. Using the simulation parameters given in Table IV, the proposed TCAM cell has been simulated using HSPICE; all reported results are at 32 and 45 nm feature sizes.

1) Average Write/Read Delay

Table V shows the simulation results for the two basic memory operations; with a reduction in feature size of the MOSFETs, delays are decreased [26]. These delays are influenced by two limiting factors: transfer error rate of the SE turnstile and the speed of the SET/MOS circuit. In the former case, the internal characteristics of the SET process affect the write delay. So, different from the conventional (CMOS-based) SRAM, there is no significant and direct improvement in delay of the write operation for "0"; this operation is mostly influenced by the SE transfer speed, not the characteristics of the MOSFET. For the latter case, the speed of the proposed SET/MOS circuit significantly affects the read delay because the highly reactive response of the SET is used in the memory to measure/sense the number of stored electrons in the "read" function.

In the worst case, the delay of the SET/MOS circuit is given by $t_d=C_{tot}V_{out}/I_o$, where t_d is the delay time, C_{tot} is the total load and inherent capacitance (including the gate and drain capacitance of SET in hybrid memory cell [26]) and I_o is the bias current. The proposed TCAM cell utilizes a SET to accomplish the "match" function by comparing the values on the Read Bit Line (RBL) and the Search Line (SL). Hence, the performance of the SET plays an important role in the matching delay, which will be investigated in more detail next.

2) Matching (Mismatching) Delay

The device characteristics of a SET require an accurate control; the proposed TCAM employs the periodic drain-current characteristics of a SET for the data matching operation, and hence deviation in the characteristics of this device can prevent the correct execution of the matching operation. From Table V, the matching delay is effective to characterize the performance of the TCAM match function (that is defined from the precharge step to the response of the match output).

The results have been categorized into two types: the matching delay (that refers to the voltage changing from low to high) and the mismatching delay, respectively. In the simulation, a low voltage level corresponds to a "Mismatch", while a high voltage level corresponds to a "Match" as output response.

In the proposed TCAM cell, the matching delay is significantly influenced by the matching SET and the internal characteristics of the cell, such as the mechanism of the phase gate for the match outcome when it stores a "Don't Care"; this mechanism is totally different from the encoding mode of a conventional TCAM cell. So, a variation on the Search Line (i.e. a change of searched data), may influence the SET as limited by its circuit features. In the HSPICE simulation of the proposed TCAM cell, the "Searched data" is always changed between "0" and "1" at the beginning of each cycle, causing a

TABLE V
HSPICE SIMULATION RESULTS FOR SINGLE TCAM CELL

Feature Size	45 nm	32 nm
Temperature (K)	300 K	300 K
Average Write Delay (ns)	9.04 ns	8.73 ns
Average Read Delay (ns)	3.06 ns	2.96 ns
Vdd (V)	2.1 V	0.9 V
Power Dissipation for Each Search Operation (W)	2.63E-9 W	4.83E-10 W
Matching Delay (0,X) (ns)	3.32 ns	3.21 ns
Matching Delay (0,1) (ns)	3.44 ns	3.31 ns
Matching Delay (1,X) (ns)	3.31 ns	3.22 ns
Matching Delay (1,0) (ns)	3.43 ns	3.33 ns
Mismatching Delay (X,0) (ns)	2.77 ns	2.69 ns
Mismatching Delay (X,1) (ns)	2.75 ns	2.68 ns
Mismatching Delay (0,1) (ns)	2.86 ns	2.73 ns
Mismatching Delay (1,0) (ns)	2.85 ns	2.71 ns

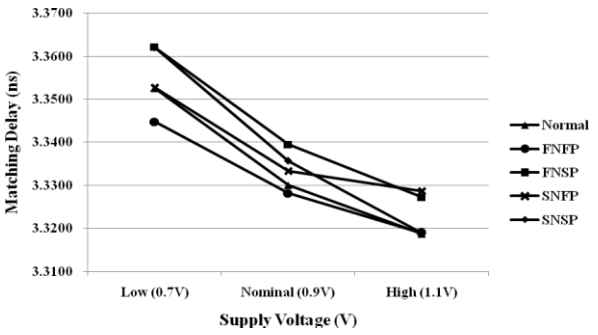

Fig. 15. Simulation results of proposed TCAM cell for match operation (0, 1) at 32nm with various technology corners and supply voltages (T=300K).

data dependency for the "Match" at the SL.

For example, following the "Match" in Cycle 1, the "Match" should be still high at the beginning of Cycle 2. With a change in "Searched data", the voltage level could decrease to a "Mismatch" with a corresponding output delay. However, the simulation results show that there is no data dependency and the memory circuit operates correctly. The operating frequency of 166 MHz as required for a correct transfer rate of the electrons in the SE turnstile (modeled at macroscopic level by HSPICE) [26] allows the proposed memory cell to process data as required by the TCAM.

3) Power Dissipation

The power dissipation of the proposed TCAM cell is related to the memory circuit and the matching SET as associated with the ML operation (the other operations do not significantly contribute to power dissipation [26]).

The dynamic power consumed by a single match line for a mismatch is due to the rising edge during the precharge process and the falling edge during the evaluation step. For a match, the power consumption associated with a single ML depends on its previous state; as in practice (for example in a network router design) only a small number of matches are encountered, then this is not significant. Simulation results show that the power dissipation of each search operation is 2630 pW and 483 pW for 45 nm and 32 nm, respectively, so decreasing with feature size.

4) Process/Voltage Variation

As the dimensions of the MOSFET scale down, variations in process, voltage, and temperature can significantly affect the correct operation of a CMOS circuit; simulation concentrates on the variations in the MOSFETs of the precharge circuitry of the proposed TCAM cell, specially the effects of variations of process and supply voltage are investigated in detail (temperature has no significant effect). Fig. 15 shows the delay for the matching operation (0,1) at a temperature of 300K at different values of technology corners and supply voltages. At these process corners, five combinations have been considered, including normal MOSFETs, fast n-fast p (FNFP), fast n-slow p (FNSP), slow n-fast p (SNFP) and slow n-slow p (SNSP). Furthermore, these combinations have been combined with three values of supply voltage (Low Voltage (0.7V), Nominal Voltage (0.9V) and High Voltage (1.1V)) to evaluate the robustness of the proposed circuit.

Fig. 15 shows that the delay degradation increases at a lower supply voltage, because at least macroscopically, this reduction affects the process of charge/discharge. Moreover at different technology process corners, simulation shows that the delay variations are limited to picoseconds. Compared to the search delay, this is not a significant issue. Therefore, these results confirm the robustness of the proposed TCAM cell and the advantage of the single electron transfer as a process that is mostly insensitive to variation.

VIII. Conclusion

This paper has presented novel designs and implementations of an SRAM cell and a TCAM cell; the SRAM cell utilizes a turnstile (to sequentially transfer SEs in and out of the storage node) and a SET/MOS circuit (to sense the charge in the storage node). One of the advantages of this cell is that by utilizing a "hybrid" implementation (i.e. using SE-based components with MOSFETs) it is compatible with CMOS technology. By utilizing hybrid designs (made of SET and CMOS devices), the proposed cells combine different operational features to improve memory performance. The operation of the proposed SRAM cell has been analyzed and simulated at the nano feature sizes of 32 and 45 nm using HSPICE compatible models; the simulation results show that the delay in the basic operations of the memory cell is mostly related to the SE transfer process and the characteristics of the turnstile. Compared to an SRAM with 45 nm MOSFETs, the SRAM at 32 nm accomplishes reduced write or read delays due to intrinsic parameters, such as gate capacitance, oxide layer capacitance and parasitic capacitance. MOSFETs have been integrated in both the SE turnstile and the SET/MOS hybrid circuit; thus, the MOSFET feature size influences the operating delays.

The proposed cell requires nearly 22% less area than a CMOS (6T) memory cell; also in terms of stability, the proposed cell shows a significant improvement in SNM for the write operation and a nearly negligible decrease for the read operation compared to the CMOS counterpart. Finally, the reduction of average power dissipation in the proposed SRAM has been mostly achieved by the lower biasing voltage and leakage encountered at 32 nm feature size and the utilization of SE driven circuitry in the design and operation of the proposed SRAM cell. While reduction in scaling will affect the characteristics of the MOS circuitry, the most significant technological challenges for high performance are with the improvement of SE based components, such as the SET and the turnstile. Issues related to the sequential and simultaneous SE transfers on the operating frequency and average delays for the two memory operations (write and read) have also been presented to show the relationship with the number of single electrons.

Moreover, a SET-based TCAM cell has been presented; this design utilizes the phase shift characteristics of the drain current of the proposed SRAM cell (consisting of a dual-gate SET and a cascode MOSFET) for ternary matching; together with a

precharge circuit, the proposed TCAM memory cell has shown by HSPICE simulation to have excellent performance.

REFERENCES

[1] B. Yu, L. Chang, S. Ahmed, et al., "FinFET scaling to 10 nm gate length," *Int. Electron. Devices Meet.* 2002; 251–254.

[2] R. Martel, V. Derycke, J. Appenzeller et al., "Carbon nanotube fieldeffect transistors and logic circuits," *ACM SIGDA DAC*, 2002.

[3] J. Redwing, T. Mayer, S. Mohney et al., "Semiconductor nanowires: building blocks for nanoscale electronics," *NSF Nanoscale Science and Engineering Grantees Conference*, December 2002.

[4] I. Amlani, A.O. Orlov, G. Toth, et al., "Digital logic gate using quantum-dot cellular automata," *Science* 284 (1999) 289–291.

[5] Y. Chen, G. Y. Jung, D.A.A. Ohlberg, et al., "Nanoscale molecularswitch crossbar circuits," *Nanotechnology* 14 (2003) 462–468.

[6] E.S. Soldatov, V.V. Khanin, A.S. Trifonov, S.P. Gubin, et al., "Room temperature molecular single-electron transistor," *Phys. Usp.* 41 (2) (1998) 202–204.

[7] G. Lientschnig, I. Weymann, P. Hadley, "Simulating hybrid circuits of single-electron transistors and field-effect transistors," *IEEE-NANO*, 2002.

[8] W. Wei and F. Lombardi, "A HSPICE model for the single-electron turnstile," *Proc. ACM GLSVLSI 2012*, pp. 221-226, 2012.

[9] T. Oya, T. Asai, and Y. Amemiya, "Stochastic resonance in an ensemble of single-electron neuromorphic devices and its application to competitive neural networks," *Chaos, Solitons Fractals*, vol. 32, pp. 855–861, 2007.

[10] K. C. Smith, "The prospects of multivalued logic: A technology and applications view," *IEEE Trans. Comput.*, vol. AC-30, no. 9, pp. 619-634, Sep. 1981.

[11] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A multiple-valued logic and memory with combined single-electron and metal-oxide-semiconductordevices," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 462-470, Feb.2003.

[12] K.K. Likharev, "Single electron transistors: electrostatic analogs of the dc squids," *IEEE Transactions on Magnetics*, vol. MAG-23, no. 2, pp. 1142-1145, March 1987.

[13] W. C. Zhang and N. J. Wu, "Nanoelectronic Circuit Architectures Based on Single-Electron Tusntiles," *2nd IEEE International Nanoelectronics Conference*, 978-1-4244-1573-1, 2008.

[14] K. Degawa, T. Aoki, T. Higuchi, "A high-density ternary content-addressable memory using single-electron transistors," *36th International Symposium on Multiple-Valued Logic*, 2006.

[15] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, "Silicon Single-Electron Devices for Logic Applications," *30th IEEE International Symposium on Multiple-Valued Logic*, pp.411, 2000.

[16] H. Inokawa and Y. Takahashi, "Experimental and simulation studies of single-electron-transistor-based multiple-valued logic," in *Proc. 33rd IEEE Int. Symp. Multiple-Valued-Logic*, May 2003, pp. 259-266.

[17] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON—a simulator for single-electron tunnel devices and circuits," *IEEE Trans. Comput. Aided Des.*, vol. 16, no. 9, pp. 937–944, Sep. 1997.

[18] R. H. Chen, Meeting Abstracts 96-2 (*The Electrochem. Soc., Pennington, Pa.*, 1996) pp. 576.

[19] H. Inokawa and Y. Takahashi, "Experimental and simulation studies of single-electron-transistor-based multiple-valued logic," in *Proc. 33th Int. Symp. Mult. Valued Logic (ISMVL)*, May, 2003, pp. 259–266.

[20] N. M. Zimmermana, E. Hourdakis, Y. Ono, A. Fujiwara, and Y. Takahashi, "Error mechanisms and rates in tunable-barrier single-electron turnstiles and charge-coupled devices," *J. Appl. Phys.*, vol. 96, pp. 5254–5266.

[21] W. C. Zhang, et al., "Transfer and Detection of Single Electrons using Metal-Oxide-Semiconductor Field-Effect-Transistors," *IEICE Trans. Electron*, vol. E90-C, pp. 943-948, May. 2007.

[22] P. R. Gray, P. J. Hurst, S. H. Lewis, and R G Meyer, "Analysis and Design of Analog Integrated Circuits (Fourth Edition ed.)," *New York: Wiley*. pp. 66–67. ISBN 0-471-32168-0, 2001.

[23] Likharev, K.K. "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions," *IBM J. Res. Dev.* 32, (1), pp. 144–156, 1998.

[24] K. Nishiguchi, H. Inokawa, Y. Ono, A. Fujiwara and Y. Takahashi, "Multilevel memory using single-electron turnstile," *Electrons Letters*, Vol. 40 No. 4, 2004.

[25] W. Zwerger and M. Scharpf, "Crossover from Coulomb blockade to ohmic conduction in small tunnel junctions," *Zeitschrift für Physik B - Condensed Matter*, 85:421-426, 1991.

[26] W. Wei, J. Han and F. Lombardi "A Hybrid Memory Cell Using Single-Electron Transfer," *Proc. IEEE/ACM Symposium on Nanoarchitectures*, pp. 16-23, San Diego, June 2011.

[27] J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits: A Design Perspective (Second Edition)," *Prentice Hall*, pp. 665, ISBN: 0130909963, 2003.

[28] A. Pavlov, M. Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test," *Springer*, pp. 40, ISBN: 1402083629, 2008.

[29] J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing Static and Dynamic Write Margin for Nanometer SRAMs," *Proc. 2008 ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 129-134, Aug 2008.

[30] S. Nakatal, H. Suzuki et al., "Increasing Static Noise Margin of Single-bit-line SRAM by Lowering Bit-line Voltage during Reading," *Proc. 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1-4, Aug 2011.

[31] H. Noda, K. Inoue, M. Kuroiwa, "A cost-efficient high-performance dynamic TCAM with pipelined hierarchical searching and shift redundancy architecture," *IEEE J. Solid-State Circuits*. vol. 40, no. 1, pp. 245-253, Jan. 2005.

[32] I. Arsovski, T. Chandler, and A. Sheikholeslami, "A ternary content-addressable memory (TCAM) based on 4T static storage and including a current-race sensing scheme," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 155–158, Jan. 2003.

[33] K. K. Likharev, "Single-electron devices and their applications," *Proc. IEEE*, Vol. 87, pp. 606 – 632, April 1999.

[34] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, " Silicon single-electron devices," *J. Phys. Condensed Matter*, Vol. 14, No. 39, pp. R995 – R1033, October 2002.

[35] K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, and Y. Takahashi, "A single-electron-transistor logic gate family and its application — part I: Basic components for binary, multiple-valued and mixed-mode logic," *Proc. 34th IEEE Int. Symp. on Multiple-Valued Logic*, pp. 262 – 268, May 2004.

[36] H. Inokawa, Y. Takahashi, K. Degawa, T. Aoki, and T. Higuchi, "A single-electron-transistor logic gate family and its application — part II: Design and simulation of a 7-3 parallel counter with a linear summation and MV latch functions," *Proc. 34th IEEE Int. Symp. on Multiple-Valued Logic*, pp. 269 – 274, May 2004.

[37] K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, and Y. Takahashi, "A single-electron-transistor logic gate family for binary, multiple-valued and mixedmode logic," *IEICE Trans. Electron.*, Vol. E87-C, No. 11, pp. 1827 – 1836, November 2004.

[38] H. Inokawa, Y. Takahashi, K. Degawa, T. Aoki, and T. Higuchi, "A simulation methodology for single-electron multiple-valued logics and its application to a latched parallel counter," *IEICE Trans. Electron.*, Vol. E87-C, No. 11, pp. 1818 – 1826, November 2004.

[39] N. Azizi and F. N. Najm, "A family of cells to reduce the soft-error-rate in Ternary-CAM," *DAC 2006*, pp. 779-784, 2006.

[40] P. F. Lin and J. B. Kuo, "A 0.8-V 128-kb four-wayset-associative two-level CMOS cache memory using two-stage wordline/bitline-oriented tag-compare(WLOTC/BLOTC) scheme," *Journal of Solid-State Circuits*, Vol. 37, pp. 1307-1317, 2002.

Wei Wei received the B.S. degree in applied physics from Beihang University, Beijing, China, in 2009, and the M.S. degree in electrical and computer engineering from Northeastern University, Boston, in 2011. He is currently working towards the Ph.D. degree in computer engineering at Northeastern University, Boston, MA.

From 2009 to present, he was involved in low-power and high performance integrated circuit design and test. His research interests include low-power digital circuit design, PVT design techniques for robust nanoscale CMOS circuits, memory physical design and methodologies and nanoscale digital device modeling.

Jie Han (S'02–M'05) received the B.Sc. degree in electronic engineering from Tsinghua University, Beijing, China, in 1999 and the Ph.D. degree from Delft University of Technology, The Netherlands, in 2004. He is currently an assistant professor in the Department of Electrical and Computer Engineering at the University of Alberta, Edmonton, AB, Canada.

His research interests include reliability and fault tolerance, nanoelectronic circuits and systems, novel computational models for nanoscale and biological applications. Dr. Han served as a Technical Program Chair in IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2012) and as a Technical Program Committee Member in several other international symposia and conferences.

Fabrizio Lombardi (M'81–SM'02-F'09) graduated in 1977 from the University of Essex (UK) with a B.Sc. (Hons.) in Electronic Engineering. In 1977 he joined the Microwave Research Unit at University College London, where he received the Master in Microwaves and Modern Optics (1978), the Diploma in Microwave Engineering (1978) and the Ph.D. from the University of London (1982).

He is currently the holder of the International Test Conference (ITC) Endowed Chair Professorship at Northeastern University, Boston. His research interests are bio-inspired and nano manufacturing/computing, VLSI design, testing, and fault/defect tolerance of digital systems. He has extensively published in these areas and coauthored/edited seven books.